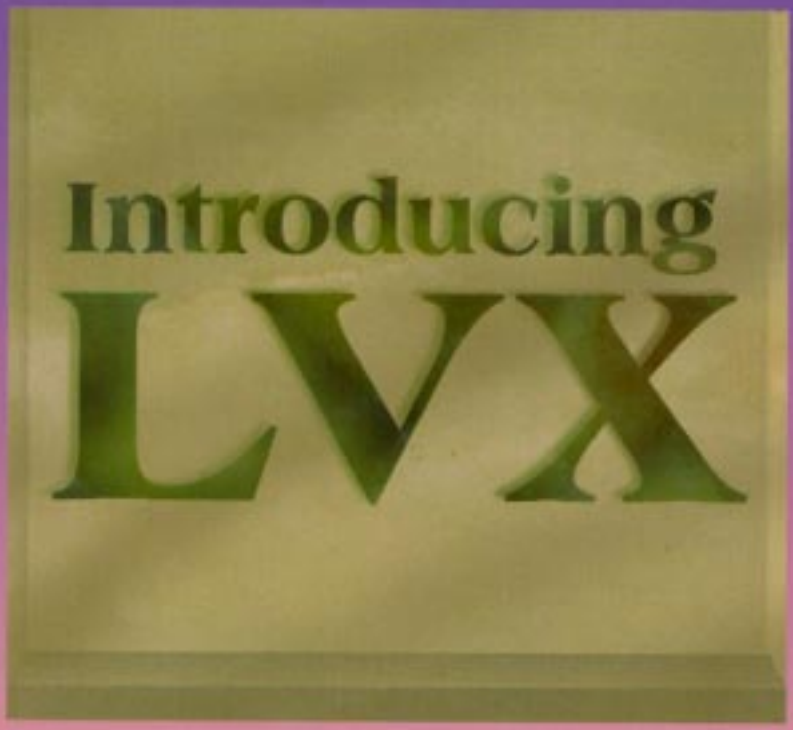
MOTOROLA

BR1492/D

LVX Data

Low-Voltage CMOS Logic



DATA SHEET CLASSIFICATIONS

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: “This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.”

Advance Information

This heading on a data sheet indicates that the device is in sampling, pre-production, or first production stages. The disclaimer at the bottom of the first page reads: “This document contains information on a new product. Specifications and information herein are subject to change without notice.”

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your Motorola Semiconductor Sales Office.

The data sheets contained in this book were the most current available as of the date of publication, July 1997.

A more current version of data sheets designated *Product Preview* or *Advance Information* may be available.

MOTOROLA

LVX Data

Low–Voltage CMOS Logic

Table of Contents

Quad 2-Input NAND Gate
With 5V-Tolerant Inputs

The MC74LVX00 is an advanced high speed CMOS 2–input NAND gate. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.1ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

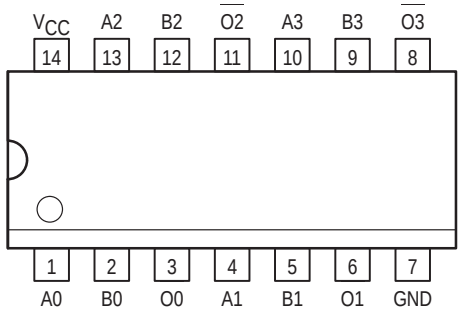


Figure 1. 14–Lead Pinout (Top View)

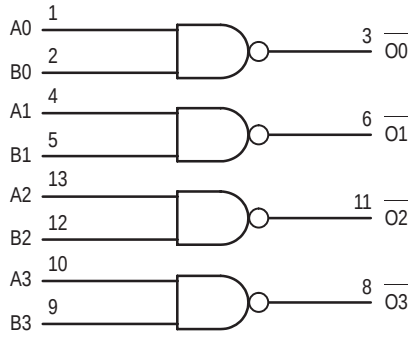
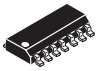


Figure 2. Logic Diagram

MC74LVX00

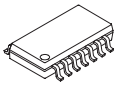
LVX

LOW–VOLTAGE CMOS



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

FUNCTION TABLE

Inputs		Outputs
An	**Bn**	**$\overline{On}$**
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			± 0.1		± 1.0	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF		5.4	10.1	1.0	12.5	ns
			C_L = 50pF		7.9	13.6	1.0	16.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		4.1	6.2	1.0	7.5	
			C_L = 50pF		6.6	9.7	1.0	11.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		19				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

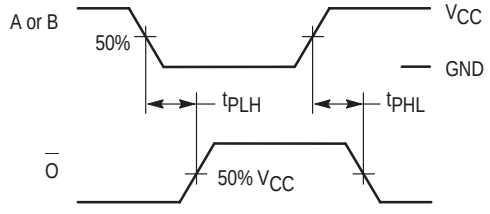
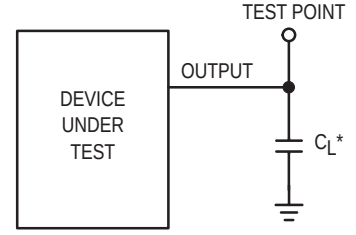


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Quad 2-Input NOR Gate
With 5V-Tolerant Inputs

The MC74LVX02 is an advanced high speed CMOS 2–input NOR gate. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.5ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

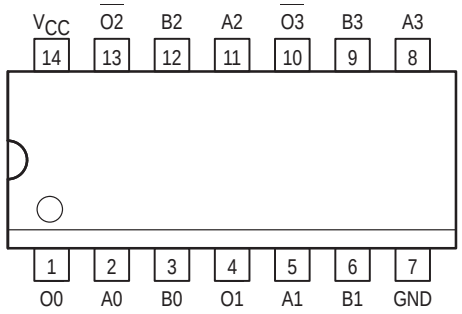


Figure 1. 14–Lead Pinout (Top View)

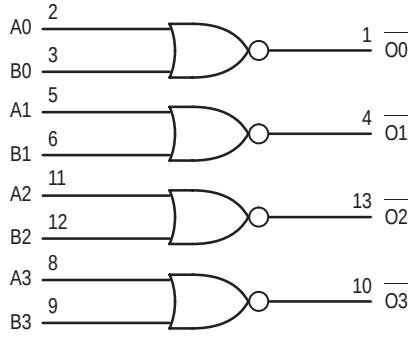
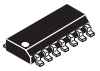


Figure 2. Logic Diagram

MC74LVX02

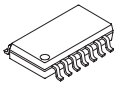
LVX

LOW–VOLTAGE CMOS



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
An	**Bn**	**$\overline{On}$**
L	L	H
L	H	L
H	L	L
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50μA I_{OH} = –50μA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF		5.9	10.7	1.0	13.5	ns
			C_L = 50pF		8.4	14.2	1.0	17.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		4.5	6.6	1.0	8.0	
			C_L = 50pF		7.0	10.1	1.0	11.5	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		15				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

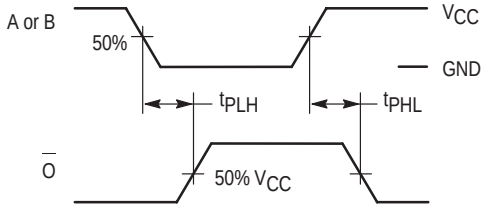
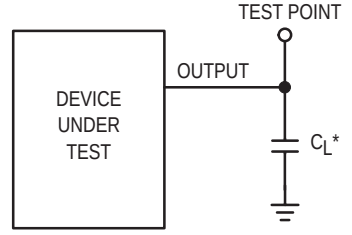


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Hex Inverter
With 5V-Tolerant Inputs

The MC74LVX04 is an advanced high speed CMOS hex inverter. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.1ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

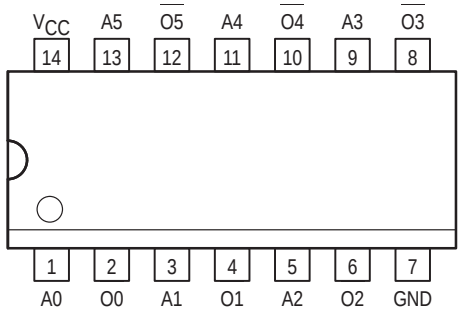


Figure 1. 14–Lead Pinout (Top View)

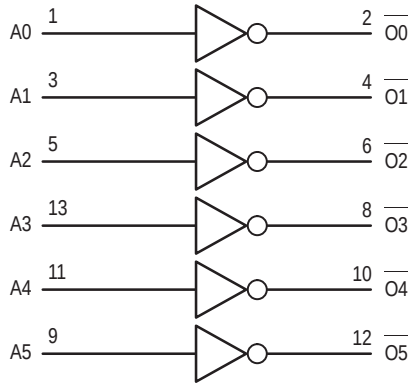
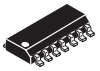


Figure 2. Logic Diagram

MC74LVX04

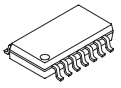
LVX

LOW–VOLTAGE CMOS



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
An On	Data Inputs Outputs

FUNCTION TABLE

An	$\overline{On}$
L H	H L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF		5.4	10.1	1.0	12.5	ns
			C_L = 50pF		7.9	13.6	1.0	16.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		4.1	6.2	1.0	7.5	
			C_L = 50pF		6.6	9.7	1.0	11.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		18				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

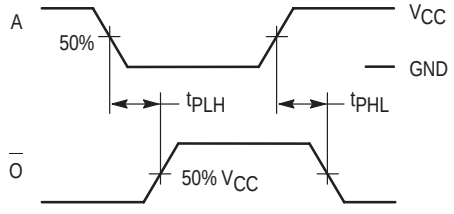
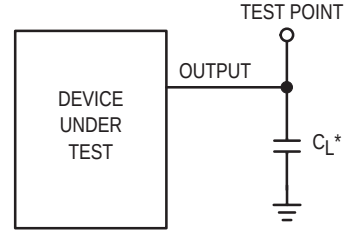


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Quad 2-Input AND Gate
With 5V-Tolerant Inputs

The MC74LVX08 is an advanced high speed CMOS 2–input AND gate. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.8ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

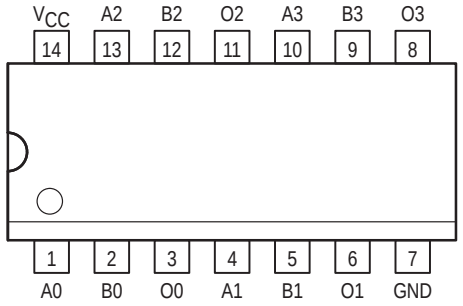


Figure 1. 14–Lead Pinout (Top View)

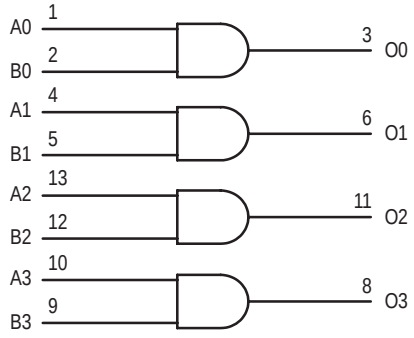
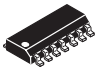


Figure 2. Logic Diagram

MC74LVX08

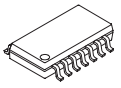
LVX

LOW–VOLTAGE CMOS



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
An	**Bn**	**On**
L	L	L
L	H	L
H	L	L
H	H	H

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF		6.3	11.4	1.0	13.5	ns
			C_L = 50pF		8.8	14.9	1.0	17.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		4.8	7.1	1.0	8.5	
			C_L = 50pF		7.3	10.6	1.0	12.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		18				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

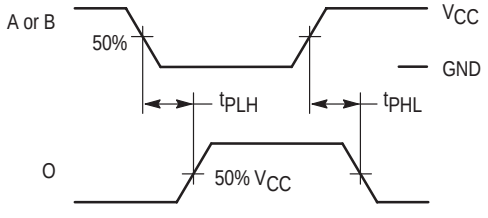
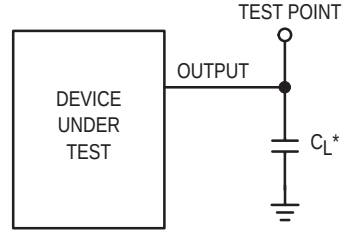


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Hex Schmitt Inverter
With 5V-Tolerant Inputs

The MC74LVX14 is an advanced high speed CMOS Schmitt inverter. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

The MC74LVX14 is pin and functionally compatible to the MC74LVX04, but the inputs have hysteresis and, with its Schmitt trigger function, can be used as a line receiver which will receive slow input signals.

- High Speed: t_{PD} = 6.8ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2µA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

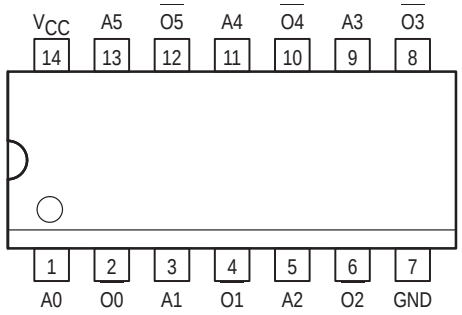


Figure 1. 14–Lead Pinout (Top View)

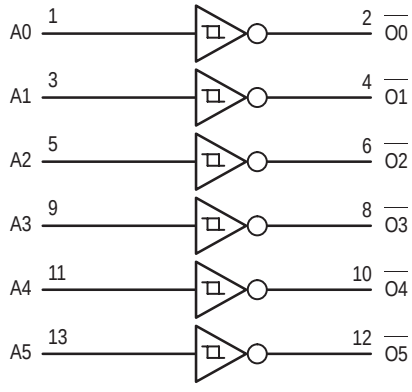
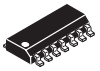


Figure 2. Logic Diagram

MC74LVX14

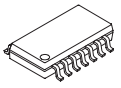
LVX

LOW–VOLTAGE CMOS



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
An	Data Inputs
On	Outputs

FUNCTION TABLE

An	$\overline{On}$
L	H
H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{T+}	Positive Threshold Voltage (Figure 5)		3.0			2.20		2.20	V
$V_{T–}$	Negative Threshold Voltage (Figure 5)		3.0	0.90			0.90		V
V_H	Hysteresis Voltage (Figure 5)		3.0	0.30		1.20	0.30	1.20	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50μA I_{OH} = –50μA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF		8.7	16.3	1.0	19.5	ns
			C_L = 50pF		11.2	19.8	1.0	23.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		6.8	10.6	1.0	12.5	
			C_L = 50pF		9.3	14.1	1.0	16.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		21				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.9	V

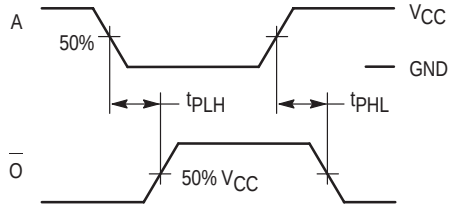
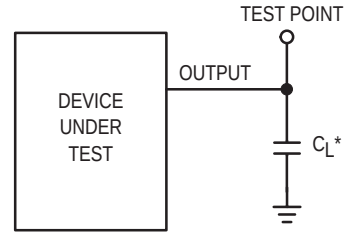


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit

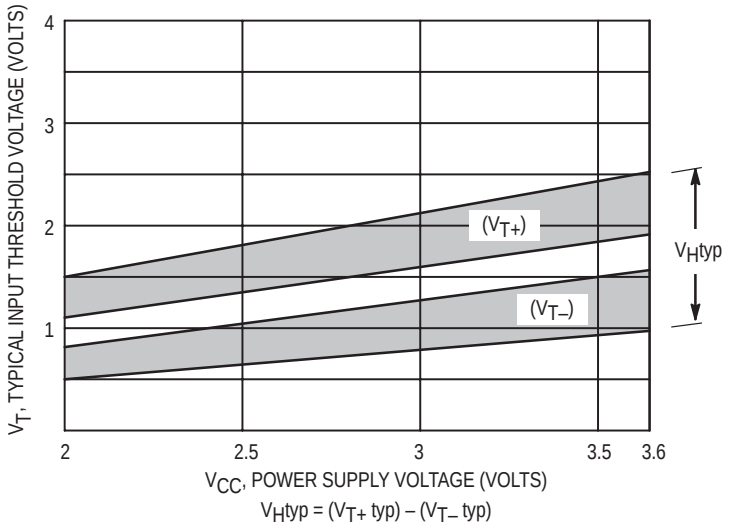


Figure 5. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

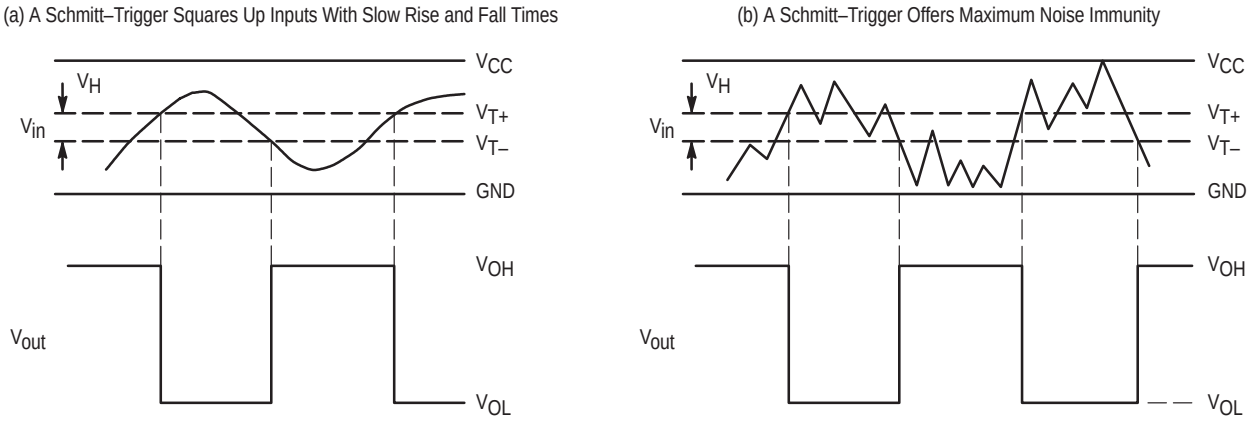


Figure 6. Typical Schmitt–Trigger Applications

Quad 2-Input OR Gate
With 5V-Tolerant Inputs

The MC74LVX32 is an advanced high speed CMOS 2–input OR gate. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.4ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

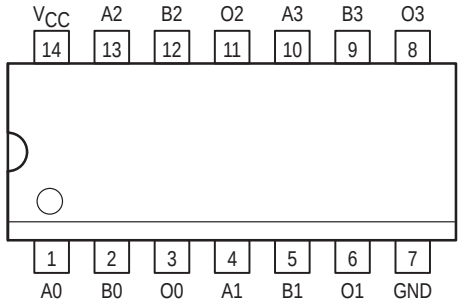


Figure 1. 14–Lead Pinout (Top View)

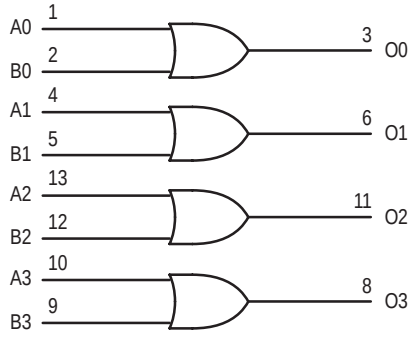
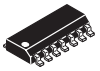


Figure 2. Logic Diagram

MC74LVX32

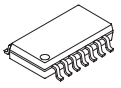
LVX

LOW–VOLTAGE CMOS



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
An	**Bn**	**On**
L	L	L
L	H	H
H	L	H
H	H	H

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50μA I_{OH} = –50μA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF		5.8	10.7	1.0	13.5	ns
			C_L = 50pF		8.3	14.2	1.0	17.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		4.4	6.6	1.0	8.0	
			C_L = 50pF		6.9	10.1	1.0	11.5	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		14				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

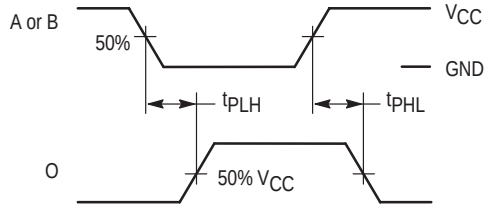
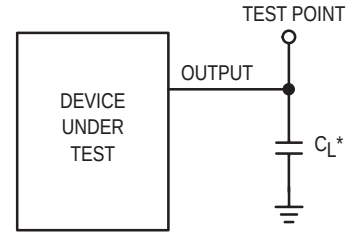


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Dual D-Type Flip-Flop with Set and Clear
With 5V-Tolerant Inputs

The MC74LVX74 is an advanced high speed CMOS D–type flip–flop. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

The signal level applied to the D input is transferred to O output during the positive going transition of the Clock pulse.

Clear ($\overline{CD}$) and Set ($\overline{SD}$) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

- High Speed: f_{max} = 145MHz (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

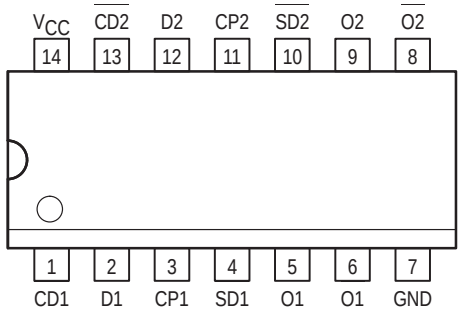


Figure 1. 14–Lead Pinout (Top View)

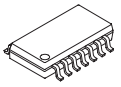
MC74LVX74

LVX

LOW–VOLTAGE CMOS

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
CP1, CP2	Clock Pulse Inputs
$\overline{D1}$, $\overline{D2}$	Data Inputs
$\overline{CD1}$, $\overline{CD2}$	Direct Clear Inputs
$\overline{SD1}$, $\overline{SD2}$	Direct Set Inputs
On, On	Outputs

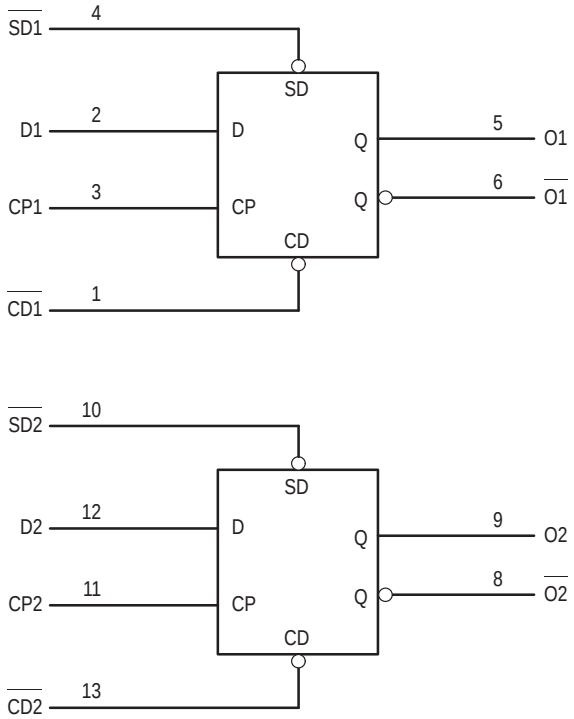


Figure 2. Logic Diagram

INPUTS				OUTPUTS		
SDn	**CDn**	**CPn**	**Dn**	**On**	**On**	**OPERATING MODE**
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	
H	H	↥	X	NC	NC	Hold

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable; ↑ = Low–to–High Transition; ↥ = Not a Low–to–High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay CP to O or O	V_{CC} = 2.7V	C_L = 15pF		7.3	15.0	1.0	18.5	ns
			C_L = 50pF		9.8	18.5	1.0	22.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.7	9.7	1.0	11.5	
			C_L = 50pF		8.2	13.2	1.0	15.0	
t_{PLH}, t_{PHL}	Propagation Delay SD or CD to O or O	V_{CC} = 2.7V	C_L = 15pF		8.4	15.6	1.0	18.5	ns
			C_L = 50pF		10.9	19.1	1.0	22.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		6.6	10.1	1.0	12.0	
			C_L = 50pF		9.1	13.6	1.0	15.5	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 2.7V	C_L = 15pF	55	135		50		MHz
			C_L = 50pF	45	60		40		
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF	95	145		80		
			C_L = 50pF	60	85		50		
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit $T_A = 25°C$	Guaranteed Limit $T_A = -40$ to $85°C$	Unit
t_w	Minimum Pulse Width, CP	2.7V	8.5	10.0	ns
		3.3V ±0.3	6.0	7.0	
t_w	Minimum Pulse Width, CD or SD	2.7V	8.5	10.0	ns
		3.3V ±0.3	6.0	7.0	
t_{su}	Minimum Setup Time, D to CP	2.7V	8.0	9.5	ns
		3.3V ±0.3	5.5	6.5	
t_h	Minimum Hold Time, D to CP	2.7V	0.5	0.5	ns
		3.3V ±0.3	0.5	0.5	
t_{rec}	Minimum Recovery Time, SD or CD to CP	2.7V	6.5	7.5	ns
		3.3V ±0.3	5.0	5.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		25				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

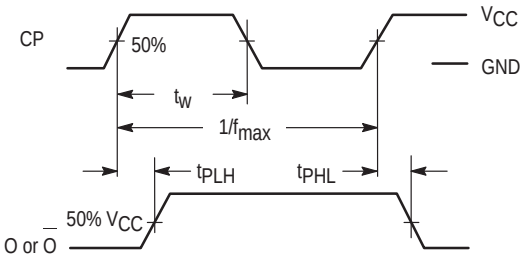


Figure 3.

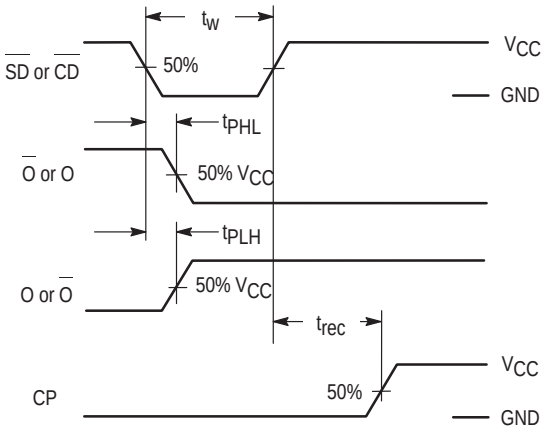


Figure 4.

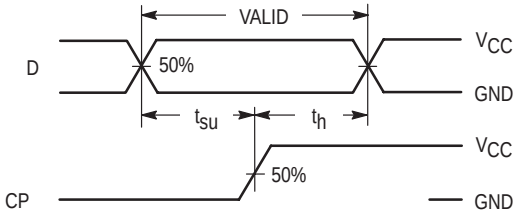
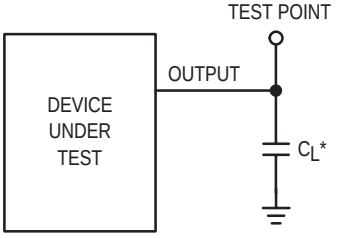


Figure 5.

TEST CIRCUIT



* Includes all probe and jig capacitance

Figure 6.

Quad 2-Input XOR Gate
With 5V-Tolerant Inputs

The MC74LVX86 is an advanced high speed CMOS 2–input Exclusive–OR gate. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 5.8ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

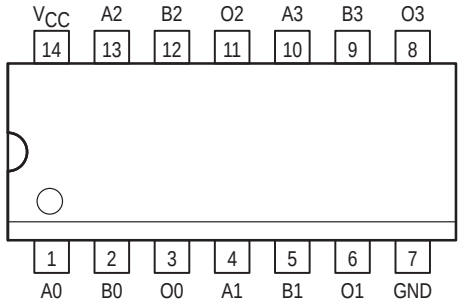


Figure 1. 14–Lead Pinout (Top View)

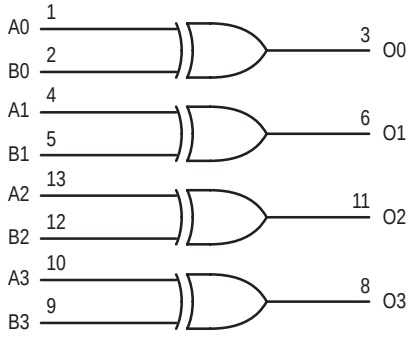
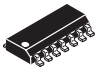


Figure 2. Logic Diagram

MC74LVX86

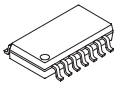
LVX

LOW–VOLTAGE CMOS



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

FUNCTION TABLE

Inputs		Outputs
An	**Bn**	**On**
L	L	L
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50μA I_{OH} = –50μA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF		7.5	14.5	1.0	17.5	ns
			C_L = 50pF		10.0	18.0	1.0	21.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.8	9.3	1.0	11.0	
			C_L = 50pF		8.3	12.8	1.0	14.5	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		18				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

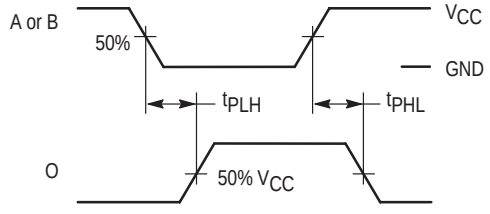
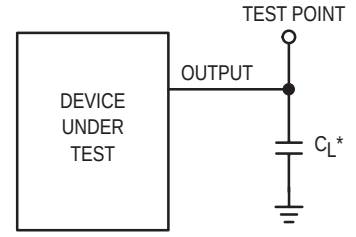


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Quad Bus Buffer
With 5V-Tolerant Inputs

The MC74LVX125 is an advanced high speed CMOS quad bus buffer. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

The MC74LVX125 requires the 3–state control input ($\overline{OE}$) to be set High to place the output into the high impedance state.

- High Speed: t_{PD} = 4.4ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4µA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

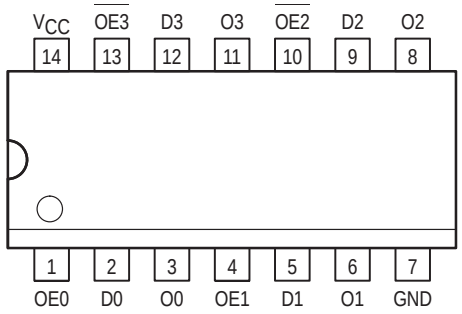


Figure 1. 14–Lead Pinout (Top View)

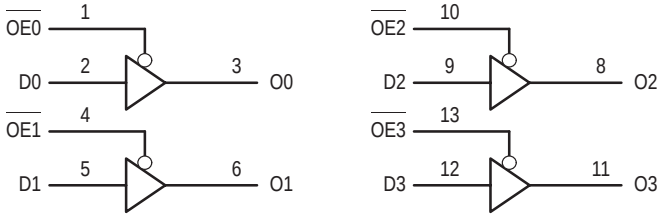


Figure 2. Logic Diagram

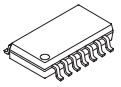
MC74LVX125

LVX

LOW–VOLTAGE CMOS

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
Dn	Data Inputs
On	3–State Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OEn}$	Dn	On
L	L	L
L	H	H
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	V_{CC} = 2.7V	C_L = 15pF		5.8	10.1	1.0	13.5	ns
			C_L = 50pF		8.3	13.6	1.0	17.0	
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 15pF		4.4	6.2	1.0	8.5	
			C_L = 50pF		6.9	9.7	1.0	12.0	
t_{PZL}, t_{PZH}	Output Enable Time OE to O	V_{CC} = 2.7V, R_L =1kΩ	C_L = 15pF		5.3	9.3	1.0	12.5	ns
			C_L = 50pF		7.8	12.8	1.0	16.0	
		$V_{CC} = 3.3 \pm 0.3$V, R_L =1kΩ	C_L = 15pF		4.0	5.6	1.0	7.5	
			C_L = 50pF		6.5	9.1	1.0	11.0	
t_{PLZ}, t_{PHZ}	Output Disable Time OE to O	V_{CC} = 2.7V, R_L =1kΩ	C_L = 50pF		10.0	15.7	1.0	19.0	MHz
		$V_{CC} = 3.3 \pm 0.3$V, R_L =1kΩ	C_L = 50pF		8.3	11.2	1.0	13.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		14				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

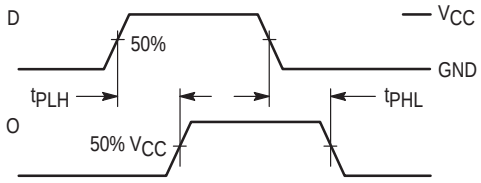


Figure 3.

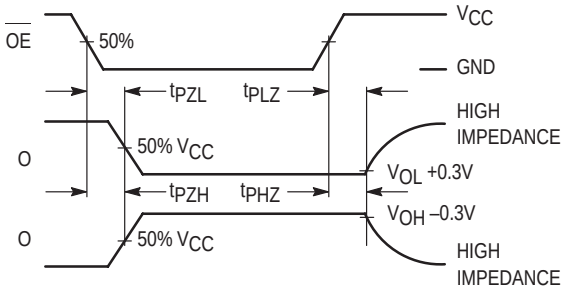
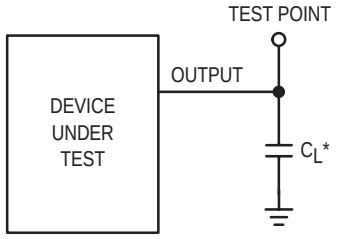


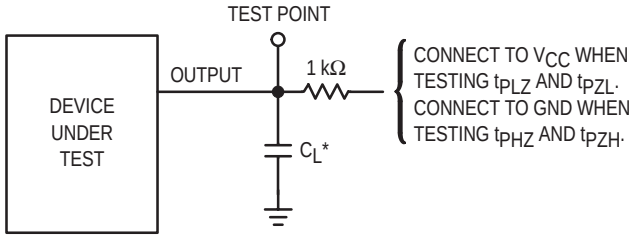
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



* Includes all probe and jig capacitance

Figure 6. Three–State Test Circuit

3-to-8 Line Decoder
With 5V-Tolerant Inputs

MC74LVX138

LVX

LOW–VOLTAGE CMOS

The MC74LVX138 is an advanced high speed CMOS 3–to–8 line decoder. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

When the device is enabled, three Binary Select inputs (A0 – A2) determine which one of the outputs (O0 – O7) will go Low. When enable input E3 is held Low or either E2 or E1 is held High, decoding function is inhibited and all outputs go high. E3, E2, and E1 inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

- High Speed: t_{PD} = 5.5ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

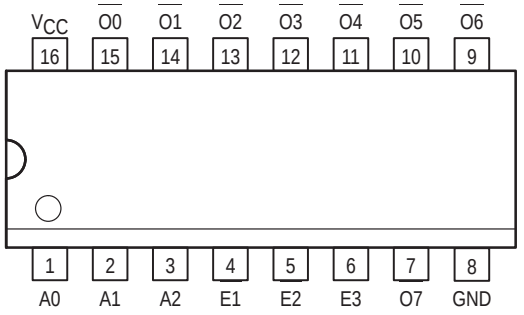
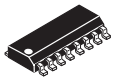
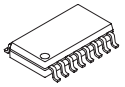


Figure 1. 16–Lead Pinout (Top View)



D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01



M SUFFIX
16–LEAD SOIC EIAJ PACKAGE
CASE 966–01

PIN NAMES

Pins	Function
A0–A2	Address Inputs
E1–E2	Enable Inputs
E3	Enable Input
O0–O7	Outputs

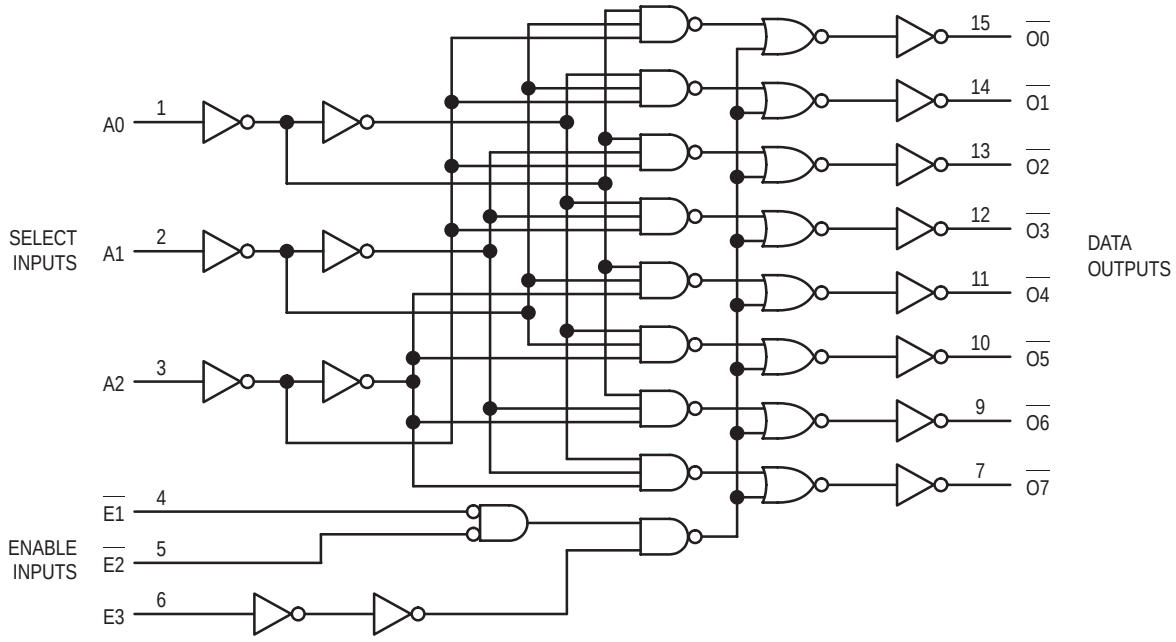


Figure 2. Logic Diagram

INPUTS						OUTPUTS							
$\overline{E1}$	$\overline{E2}$	E3	A0	A1	A2	$\overline{O0}$	$\overline{O1}$	$\overline{O2}$	$\overline{O3}$	$\overline{O4}$	$\overline{O5}$	$\overline{O6}$	$\overline{O7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level and Transitions Are Acceptable; For I_{CC} reasons, DO NOT FLOAT Inputs

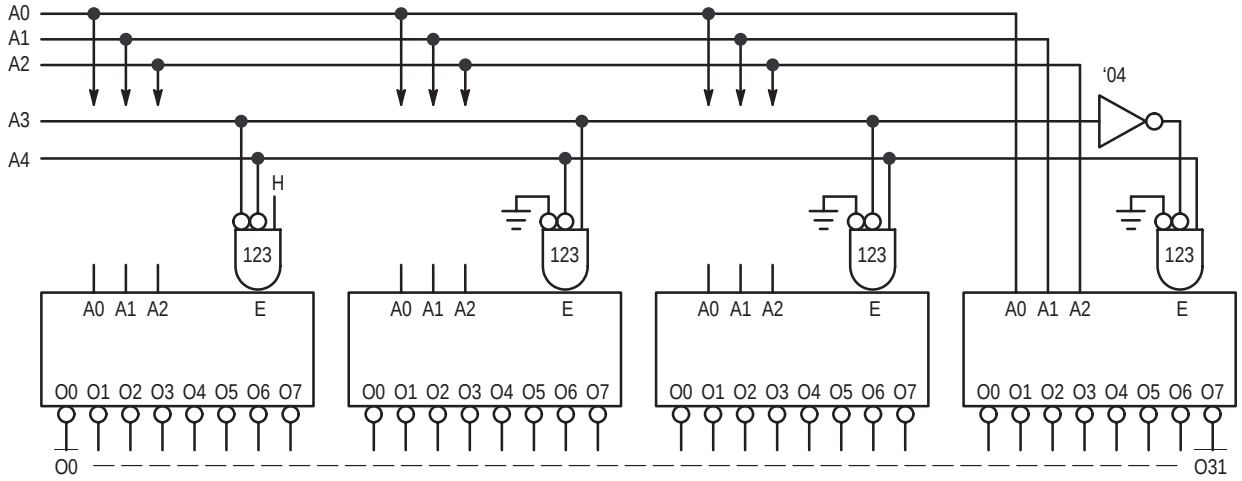


Figure 3. Expansion to 1–of–32 Decoding

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50μA I_{OH} = –50μA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	$V_{CC} = 2.7V$	$C_L = 15pF$		7.1	13.8	1.0	16.5	ns
			$C_L = 50pF$		9.6	17.3	1.0	20.0	
		$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$		5.5	8.8	1.0	10.5	
			$C_L = 50pF$		8.0	12.3	1.0	14.0	
t_{PLH}, t_{PHL}	Propagation Delay E3 to O	$V_{CC} = 2.7V$	$C_L = 15pF$		8.7	16.3	1.0	19.5	ns
			$C_L = 50pF$		11.2	19.8	1.0	23.0	
		$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$		6.8	10.6	1.0	12.5	
			$C_L = 50pF$		9.3	14.1	1.0	16.0	
t_{PLH}, t_{PHL}	Propagation Delay E1 or E2 to O	$V_{CC} = 2.7V$	$C_L = 15pF$		8.8	16.0	1.0	18.5	ns
			$C_L = 50pF$		11.3	19.5	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$		6.9	10.4	1.0	11.5	
			$C_L = 50pF$		9.4	13.9	1.0	15.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	$V_{CC} = 2.7V$	$C_L = 50pF$			2.5		2.5	ns
		$V_{CC} = 3.3 \pm 0.3V$	$C_L = 50pF$			2.5		2.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		34				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50pF$, $V_{CC} = 3.3V$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

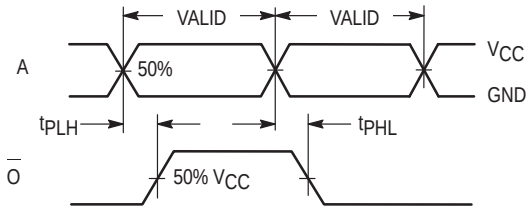


Figure 4.

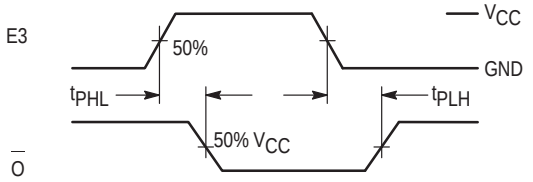


Figure 5.

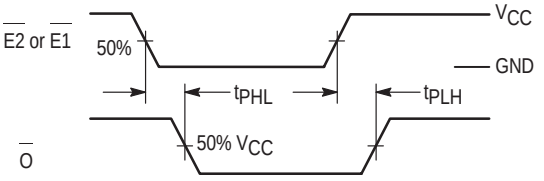
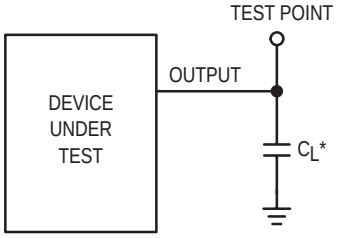


Figure 6.

TEST CIRCUIT



* Includes all probe and jig capacitance

Figure 7. Test Circuit

Quad 2-Channel Multiplexer
With 5V-Tolerant Inputs

The MC74LVX157 is an advanced high speed CMOS quad 2–channel multiplexer. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

It consists of four 2–input digital multiplexers with common select (S) and enable (E) inputs. When E is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the I0n or I1n inputs get routed to the corresponding Zn outputs.

- High Speed: t_{PD} = 5.1ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

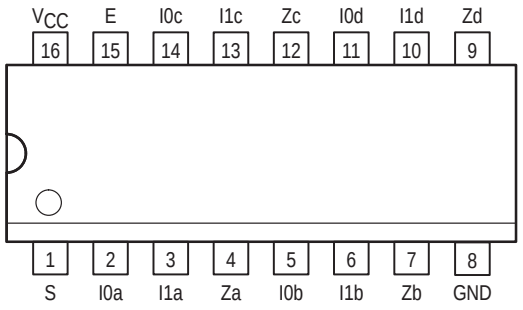


Figure 1. 16–Lead Pinout (Top View)

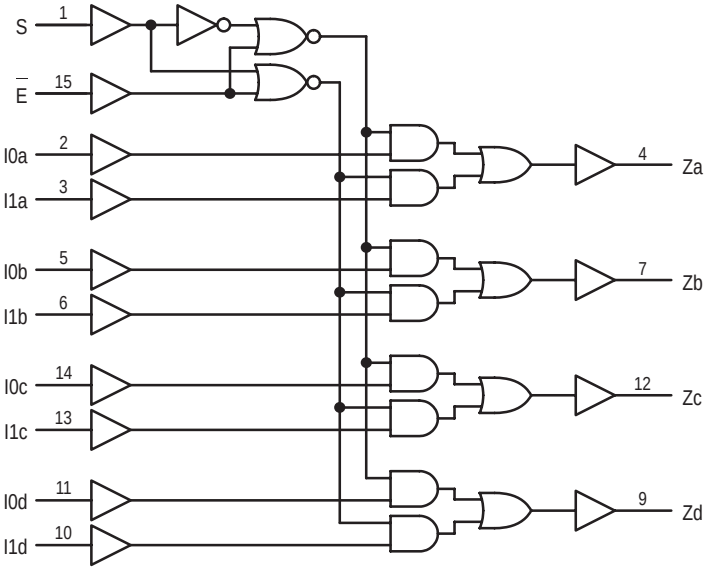
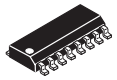


Figure 2. Logic Diagram

MC74LVX157

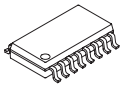
LVX

LOW–VOLTAGE CMOS



D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01



M SUFFIX
16–LEAD SOIC EIAJ PACKAGE
CASE 966–01

PIN NAMES

Pins	Function
I0n	Source 0 Data Inputs
I1n	Source 1 Data Inputs
E	Enable Input
S	Select Input
Zn	Outputs

TRUTH TABLE

INPUTS				OUTPUT
$\overline{E}$	S	I0n	I1n	Zn
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level ; For I_{CC} Reasons DO NOT FLOAT Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50μA I_{OH} = –50μA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15pF		6.6	12.5	1.0	15.5	ns
			C_L = 50pF		9.1	16.0	1.0	19.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.1	7.9	1.0	9.5	
			C_L = 50pF		7.6	11.4	1.0	13.0	
t_{PLH}, t_{PHL}	Propagation Delay, S to Zn	V_{CC} = 2.7V	C_L = 15pF		8.9	16.9	1.0	20.5	ns
			C_L = 50pF		11.4	20.4	1.0	24.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		7.0	11.0	1.0	13.0	
			C_L = 50pF		9.5	14.5	1.0	16.5	
t_{PLH}, t_{PHL}	Propagation Delay, E to Zn	V_{CC} = 2.7V	C_L = 15pF		9.1	17.6	1.0	20.5	ns
			C_L = 50pF		11.6	21.1	1.0	24.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		7.2	11.5	1.0	13.5	
			C_L = 50pF		9.7	15.0	1.0	17.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		20				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

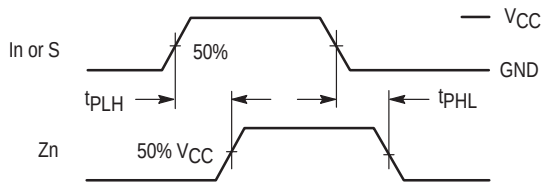


Figure 3.

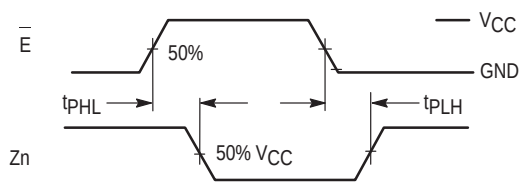
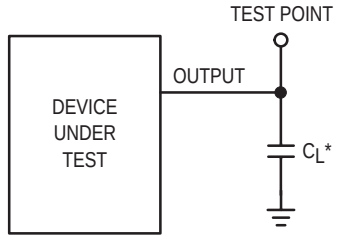


Figure 4.

TEST CIRCUIT



* Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit

Octal Bus Buffer
Inverting With 5V-Tolerant Inputs

The MC74LVX240 is an advanced high speed CMOS inverting 3–state octal bus buffer and has two active low output enables. It is also designed to work with 3–state memory address drivers, etc. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.3ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

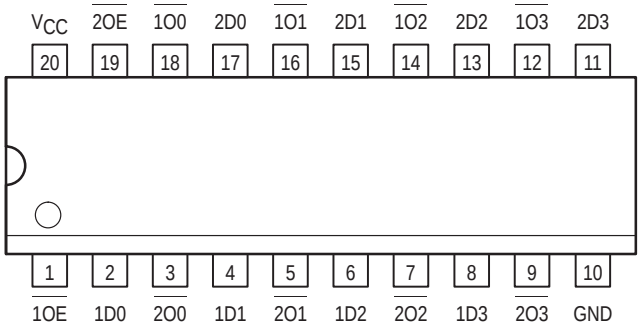


Figure 1. 20–Lead Pinout (Top View)

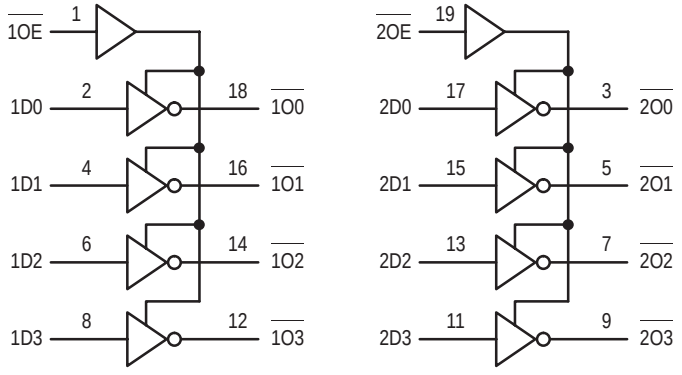
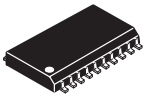


Figure 2. Logic Diagram

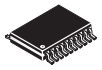
MC74LVX240

LVX

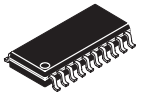
LOW–VOLTAGE CMOS



DW SUFFIX
20–LEAD SOIC PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02



M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

PIN NAMES

Pins	Function
$\overline{\text{nOE}}$	Output Enable Inputs
1Dn, 2Dn	Data Inputs
1On, 2On	3–State Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{\text{1OE}}$, $\overline{\text{2OE}}$	1Dn, 2Dn	$\overline{\text{1On}}$, $\overline{\text{2On}}$
L	L	L
L	H	H
H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	V_{CC} = 2.7V	C_L = 15pF		5.7	10.1	1.0	12.5	ns
			C_L = 50pF		8.2	13.6	1.0	16.0	
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 15pF		4.3	6.2	1.0	7.5	
			C_L = 50pF		6.8	9.7	1.0	11.0	
t_{PZL}, t_{PZH}	Output Enable Time to High and Low Level	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 15pF		7.1	13.8	1.0	16.5	ns
			C_L = 50pF		9.6	17.3	1.0	20.0	
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 15pF		5.5	8.8	1.0	10.5	
			C_L = 50pF		8.0	12.3	1.0	14.0	
t_{PLZ}, t_{PHZ}	Output Disable Time From High and Low Level	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 50pF		11.6	16.0	1.0	19.0	ns
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 50pF		9.7	11.4	1.0	13.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		19				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.5	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

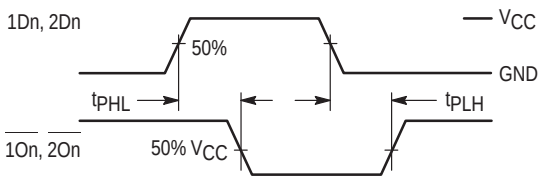


Figure 3.

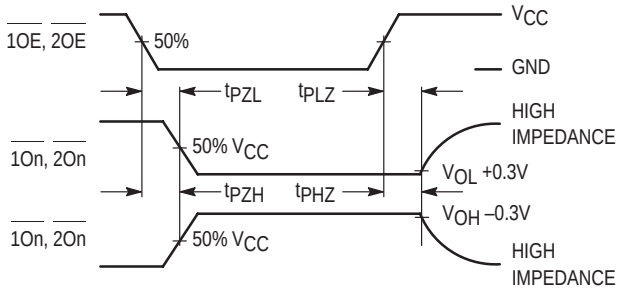
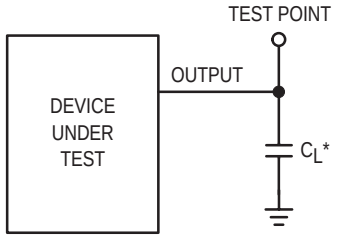


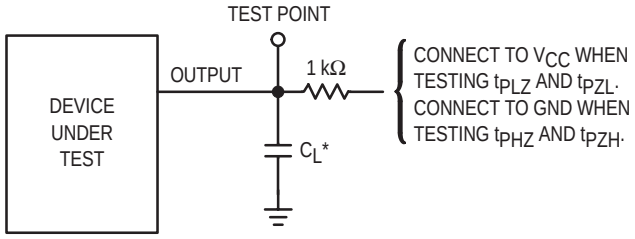
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



* Includes all probe and jig capacitance

Figure 6. Three–State Test Circuit

Octal Bus Buffer
With 5V-Tolerant Inputs

The MC74LVX244 is an advanced high speed CMOS non–inverting 3–state octal bus buffer and has two active low output enables. It is also designed to work with 3–state memory address drivers, etc. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.7ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

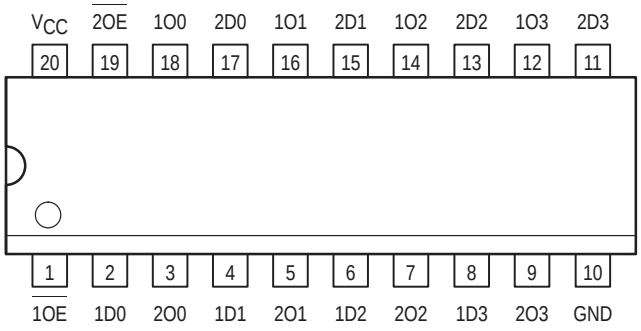


Figure 1. 20–Lead Pinout (Top View)

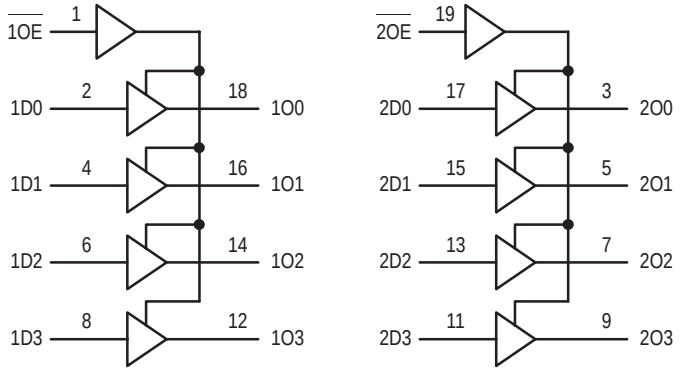
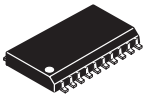


Figure 2. Logic Diagram

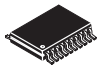
MC74LVX244

LVX

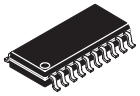
LOW–VOLTAGE CMOS



DW SUFFIX
20–LEAD SOIC PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02



M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

PIN NAMES

Pins	Function
$\overline{\text{nOE}}$	Output Enable Inputs
1Dn, 2Dn	Data Inputs
1On, 2On	3–State Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{\text{1OE}}$, $\overline{\text{2OE}}$	1Dn, 2Dn	1On, 2On
L	L	L
L	H	H
H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	V_{CC} = 2.7V	C_L = 15pF		6.1	11.4	1.0	13.5	ns
			C_L = 50pF		8.6	14.9	1.0	17.0	
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 15pF		4.7	7.1	1.0	8.5	
			C_L = 50pF		7.2	10.6	1.0	12.0	
t_{PZL}, t_{PZH}	Output Enable Time to High and Low Level	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 15pF		7.1	13.8	1.0	16.5	ns
			C_L = 50pF		9.6	17.3	1.0	20.0	
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 15pF		5.5	8.8	1.0	10.5	
			C_L = 50pF		8.0	12.3	1.0	14.0	
t_{PLZ}, t_{PHZ}	Output Disable Time From High and Low Level	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 50pF		11.6	16.0	1.0	19.0	ns
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 50pF		9.7	11.4	1.0	13.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		19				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.5	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

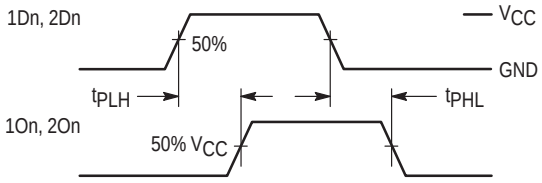


Figure 3.

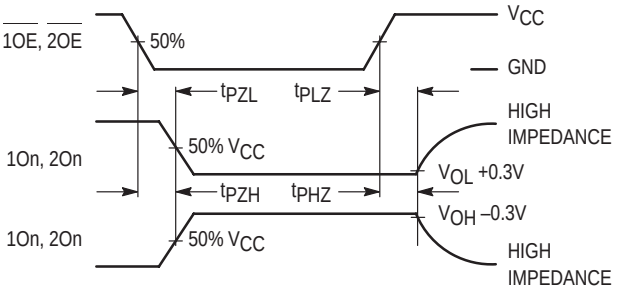
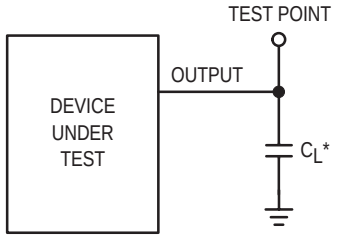


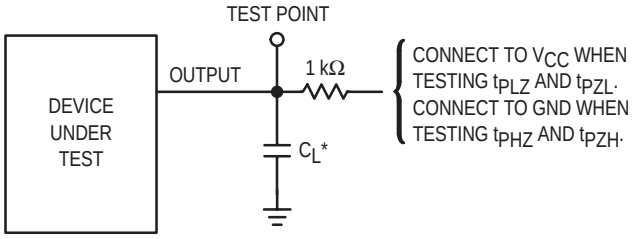
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



* Includes all probe and jig capacitance

Figure 6. Three–State Test Circuit

Octal Bus Transceiver
With 5V-Tolerant Inputs

MC74LVX245

LVX

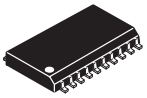
LOW–VOLTAGE CMOS

The MC74LVX245 is an advanced high speed CMOS octal bus transceiver.

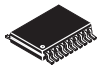
It is intended for two–way asynchronous communication between data buses. The direction of data transmission is determined by the level of the T/R input. The output enable pin (OE) can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

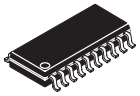
- High Speed: t_{PD} = 4.7ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V



DW SUFFIX
20–LEAD SOIC PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02



M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

APPLICATION NOTES

1. Do not force a signal on an I/O pin when it is an active output, damage may occur.
2. All floating (high impedence) input or I/O pins must be fixed by means of pull up or pull down resistors or bus terminator ICs.
3. A parasitic diode is formed between the bus and V_{CC} terminals. Therefore, the LVX245 cannot be used to interface 5V to 3V systems directly.

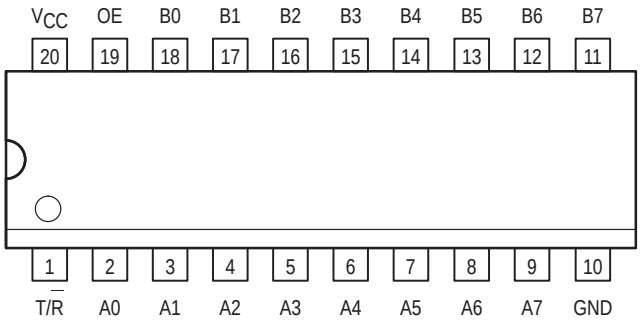


Figure 1. 20–Lead Pinout (Top View)

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
T/R	Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State Outputs
B0–B7	Side B 3–State Inputs or 3–State Outputs

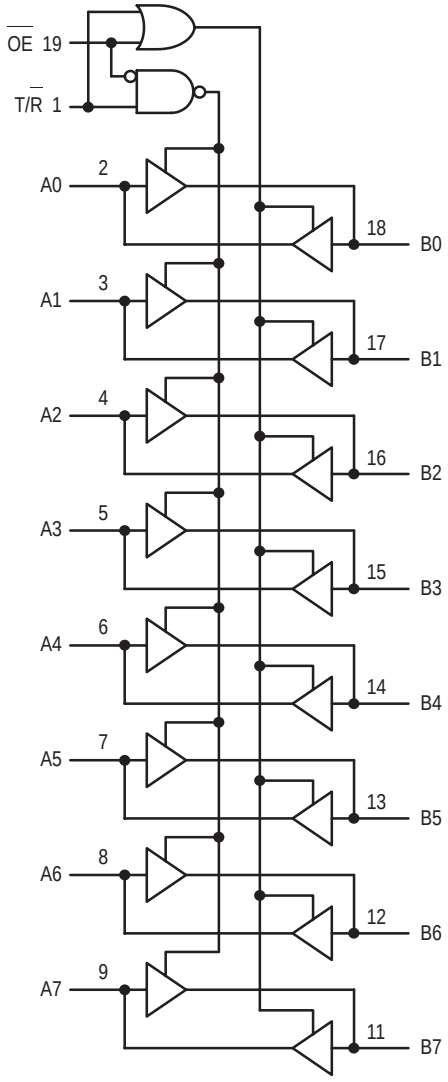


Figure 2. Logic Diagram

INPUTS		OPERATING MODE Non–Inverting
OE	T/R	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage (T/R, $\overline{OE}$)	–0.5 to +7.0	V
$V_{I/O}$	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage (T/R, $\overline{OE}$)	0	5.5	V
$V_{I/O}$	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND (T/R, $\overline{OE}$)	3.6			±0.1		±1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	V_{CC} = 2.7V	C_L = 15pF		6.1	10.7	1.0	13.5	ns
			C_L = 50pF		8.6	14.2	1.0	17.0	
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 15pF		4.7	6.6	1.0	8.0	
			C_L = 50pF		7.2	10.1	1.0	11.5	
t_{PZL}, t_{PZH}	Output Enable Time to High and Low Level	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 15pF		9.0	16.9	1.0	20.5	ns
			C_L = 50pF		11.5	20.4	1.0	24.0	
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 15pF		7.1	11.0	1.0	13.0	
			C_L = 50pF		9.6	14.5	1.0	16.5	
t_{PLZ}, t_{PHZ}	Output Disable Time From High and Low Level	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 50pF		11.5	18.0	1.0	21.0	ns
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 50pF		9.6	12.8	1.0	14.5	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance (T/R, OE)		4	10		10	pF
$C_{I/O}$	Maximum Three–State I/O Capacitance		8				pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		21				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.5	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

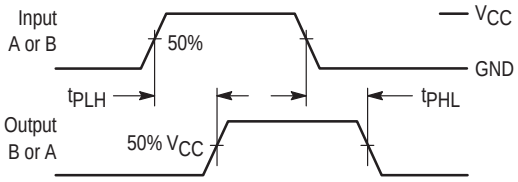


Figure 3.

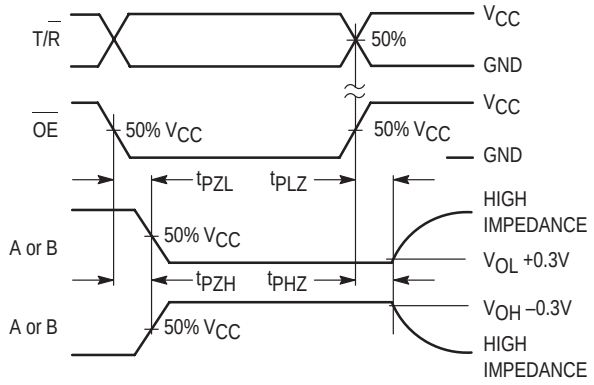
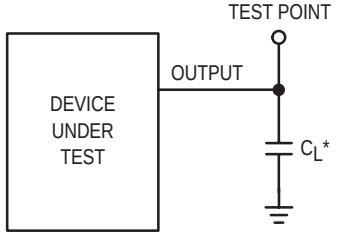


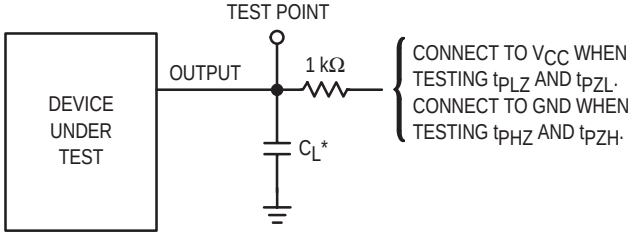
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



* Includes all probe and jig capacitance

Figure 6. Three–State Test Circuit

Octal D-Type Latch with 3-State Outputs
With 5V-Tolerant Inputs

MC74LVX373

LVX

LOW–VOLTAGE CMOS

The MC74LVX373 is an advanced high speed CMOS octal latch with 3–state outputs. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

This 8–bit D–type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

- High Speed: t_{PD} = 5.8ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

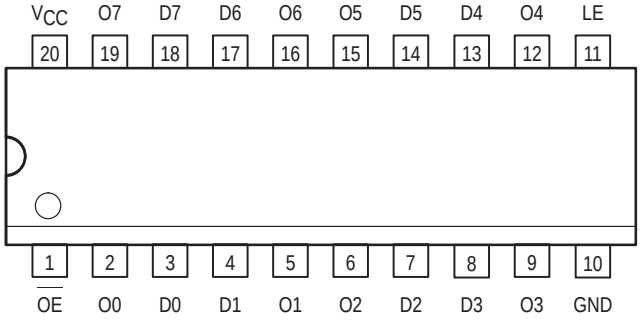
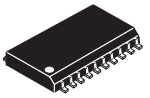
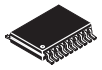


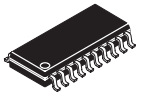
Figure 1. 20–Lead Pinout (Top View)



DW SUFFIX
20–LEAD SOIC PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02



M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

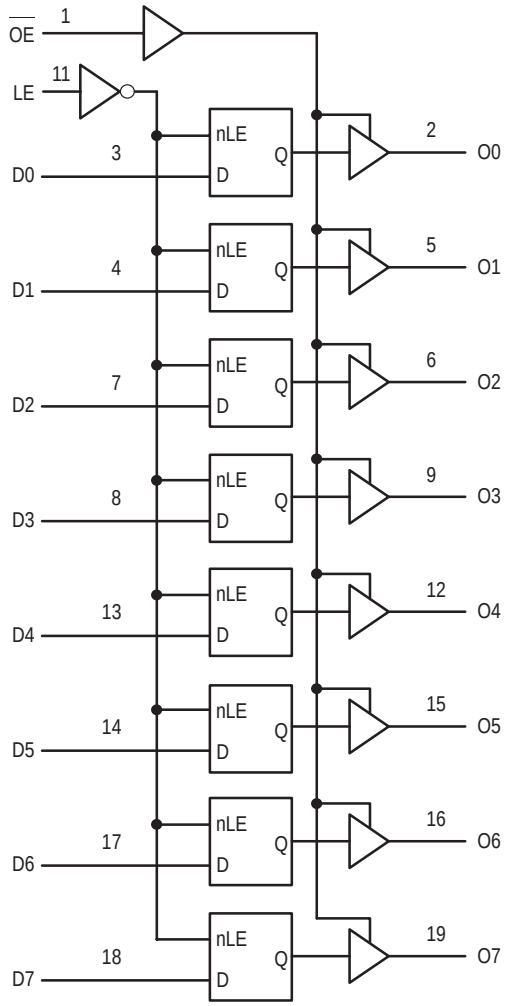


Figure 2. Logic Diagram

INPUTS			OUTPUTS	
$\overline{OE}$	LE	Dn	On	OPERATING MODE
L L	H H	H L	H L	Transparent (Latch Disabled); Read Latch
L L	L L	h l	H L	Latched (Latch Enabled) Read Latch
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H H	H H	H L	Z Z	Transparent (Latch Disabled); Disabled Outputs
H H	L L	h l	Z Z	Latched (Latch Enabled); Disabled Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition; NC = No Change, State Prior to the Latch Enable High–to–Low Transition; X = High or Low Voltage Level or Transitions are Acceptable; Z = High Impedance State; For I_{CC} Reasons DO NOT FLOAT Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay D to O	V_{CC} = 2.7V	C_L = 15pF		7.5	14.5	1.0	17.5	ns
			C_L = 50pF		10.0	18.0	1.0	21.0	
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 15pF		5.8	9.3	1.0	11.0	
			C_L = 50pF		8.3	12.8	1.0	14.5	
t_{PLH}, t_{PHL}	Propagation Delay LE to O	V_{CC} = 2.7V	C_L = 15pF		7.7	15.0	1.0	18.5	ns
			C_L = 50pF		10.2	18.5	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 15pF		6.0	9.7	1.0	11.5	
			C_L = 50pF		8.5	13.2	1.0	15.0	
t_{PZL}, t_{PZH}	Output Enable Time OE to O	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 15pF		7.7	15.0	1.0	18.5	ns
			C_L = 50pF		10.2	18.5	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 15pF		6.0	9.7	1.0	11.5	
			C_L = 50pF		8.5	13.2	1.0	15.0	
t_{PLZ}, t_{PHZ}	Output Disable Time OE to O	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 50pF		9.8	18.0	1.0	21.0	ns
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 50pF		8.2	12.8	1.0	14.5	
t_{OSHL}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
t_{OSLH}		$V_{CC} = 3.3 \pm 0.3$V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		27				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.5	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		6.5 5.0	7.5 5.0	ns
t_{su}	Minimum Setup Time, D to LE	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		6.0 4.0	6.0 4.0	ns
t_h	Minimum Hold Time, D to LE	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		1.0 1.0	1.0 1.0	ns

SWITCHING WAVEFORMS

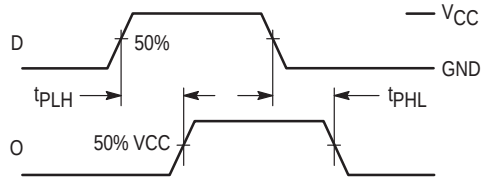


Figure 3.

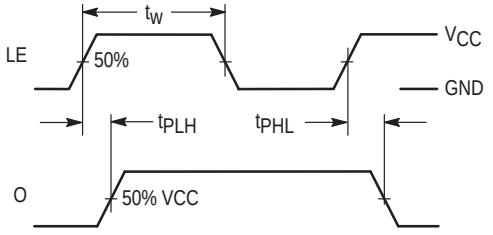


Figure 4.

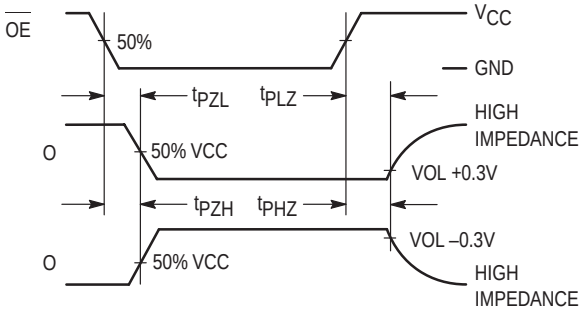


Figure 5.

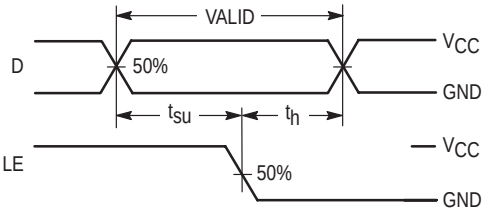
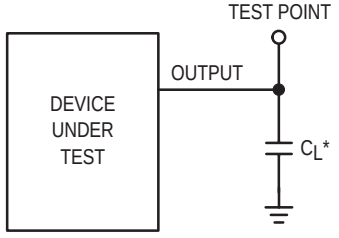


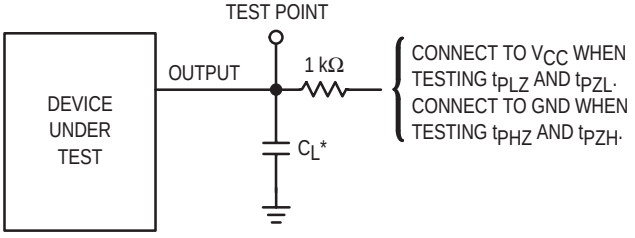
Figure 6.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 7. Propagation Delay Test Circuit



* Includes all probe and jig capacitance

Figure 8. Three–State Test Circuit

Octal D-Type Flip-Flop with 3-State Outputs
With 5V-Tolerant Inputs

MC74LVX374

LVX

LOW–VOLTAGE CMOS

The MC74LVX374 is an advanced high speed CMOS octal D–type flip–flop with 3–state outputs. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

This 8–bit D–type flip–flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

- High Speed: f_{max} = 160MHz (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

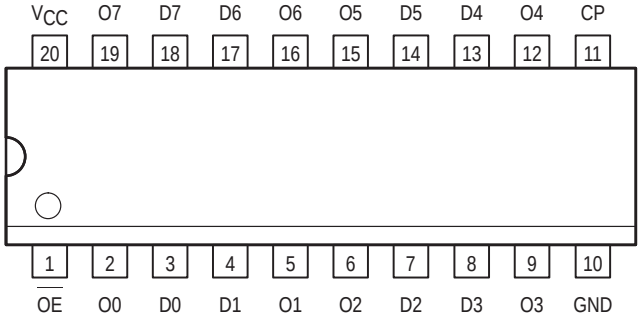
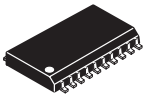
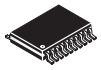


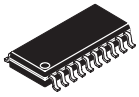
Figure 1. 20–Lead Pinout (Top View)



DW SUFFIX
20–LEAD SOIC PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02



M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
CP	Clock Pulse Input
D0–D7	Data Inputs
O0–O7	3–State Outputs

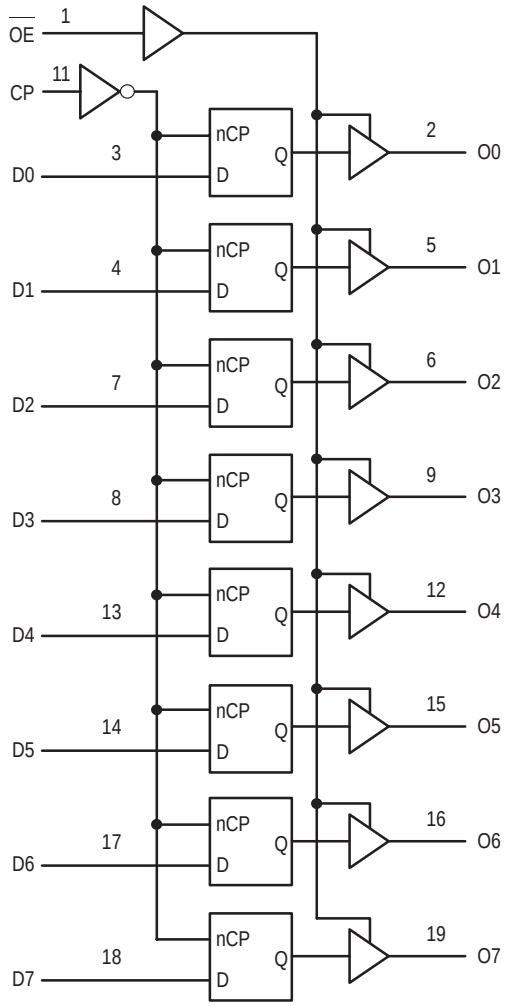


Figure 2. Logic Diagram

INPUTS			OUTPUTS	OPERATING MODE
OE	**CP**	**Dn**	**On**	
L L	↑ ↑	l h	L H	Load and Read Register
L	↥	X	NC	Hold and Read Register
H	↥	X	Z	Hold and Disable Outputs
H H	↑ ↑	l h	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change, State Prior to Low–to–High Clock Transition; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↑ = Low–to–High Transition; ↥ = Not a Low–to–High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 2.7V	C_L = 15pF	60	115		50		MHz
			C_L = 50pF	45	60		40		
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 15pF	100	160		85		
			C_L = 50pF	60	95		55		
t_{PLH}, t_{PHL}	Propagation Delay CP to O	V_{CC} = 2.7V	C_L = 15pF		8.5	16.3	1.0	19.5	ns
			C_L = 50pF		11.0	19.8	1.0	23.0	
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 15pF		6.7	10.6	1.0	12.5	
			C_L = 50pF		9.2	14.1	1.0	16.0	
t_{PZL}, t_{PZH}	Output Enable Time OE to O	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 15pF		7.6	14.5	1.0	17.5	ns
			C_L = 50pF		10.1	18.0	1.0	21.0	
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 15pF		5.9	9.3	1.0	11.0	
			C_L = 50pF		8.4	12.8	1.0	14.5	
t_{PLZ}, t_{PHZ}	Output Disable Time OE to O	V_{CC} = 2.7V, R_L = 1kΩ	C_L = 50pF		11.5	18.5	1.0	22.0	ns
		$V_{CC} = 3.3 \pm 0.3$V, R_L = 1kΩ	C_L = 50pF		9.6	13.2	1.0	15.0	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3$V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		32				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.5	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
t_w	Minimum Pulse Width, CP	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		7.5 5.0	8.0 5.5	ns
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		6.5 4.5	6.5 4.5	ns
t_h	Minimum Hold Time, D to CP	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		2.0 2.0	2.0 2.0	ns

SWITCHING WAVEFORMS

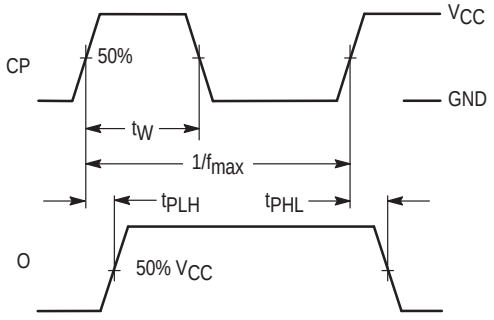


Figure 3.

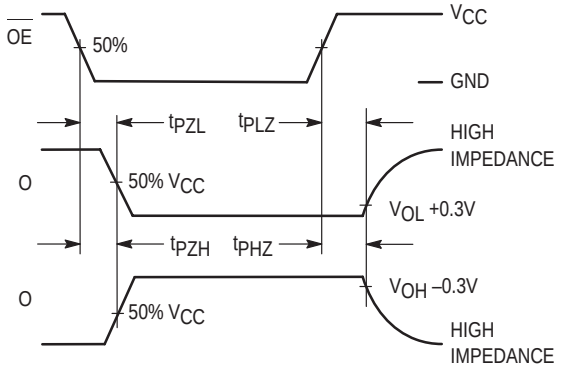


Figure 4.

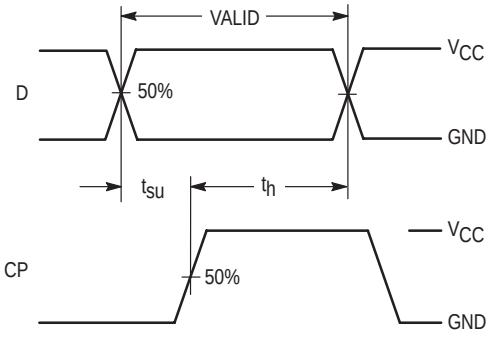
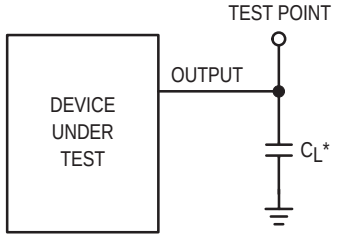


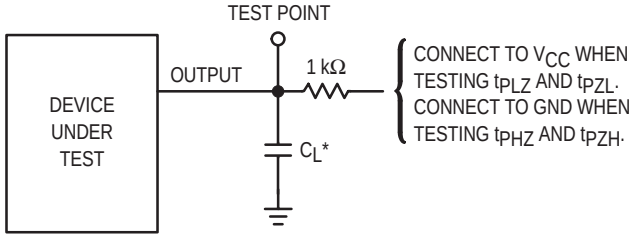
Figure 5.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 6. Propagation Delay Test Circuit



* Includes all probe and jig capacitance

Figure 7. Three–State Test Circuit

Octal D-Type Latch with 3-State Outputs
With 5V-Tolerant Inputs

MC74LVX573

LVX

LOW–VOLTAGE CMOS

The MC74LVX573 is an advanced high speed CMOS octal latch with 3–state outputs. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

This 8–bit D–type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

- High Speed: t_{PD} = 6.4ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

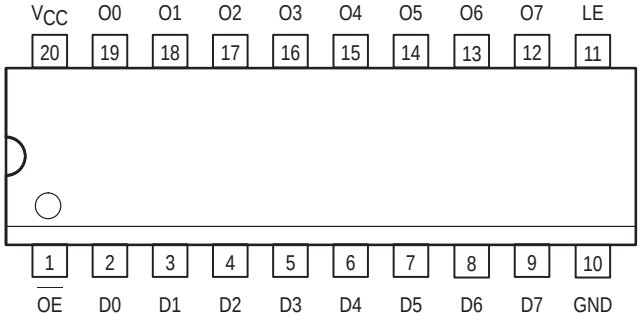
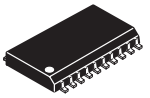
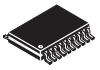


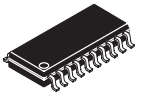
Figure 1. 20–Lead Pinout (Top View)



DW SUFFIX
20–LEAD SOIC PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02



M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

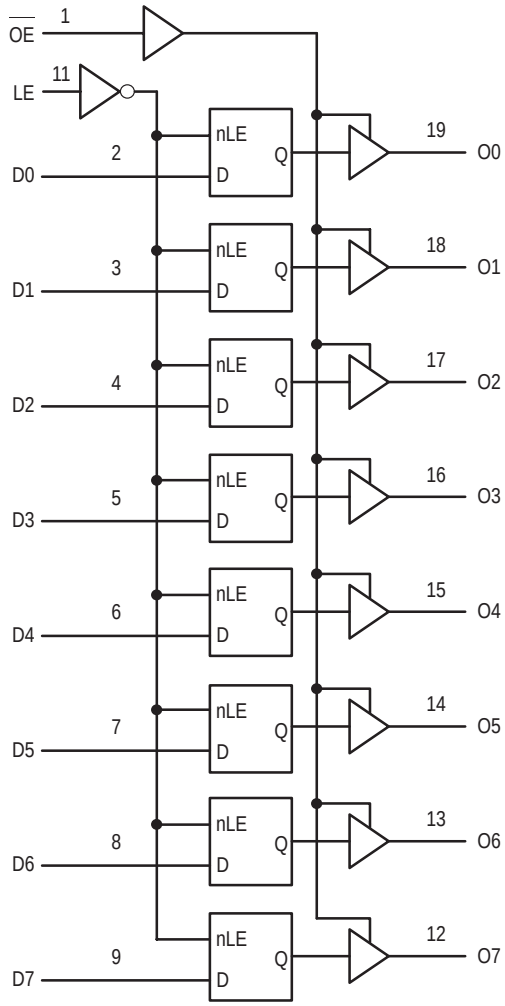


Figure 2. Logic Diagram

INPUTS			OUTPUTS	OPERATING MODE
OE	LE	Dn	On	
L L	H H	H L	H L	Transparent (Latch Disabled); Read Latch
L L	L L	h l	H L	Latched (Latch Enabled) Read Latch
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H H	H H	H L	Z Z	Transparent (Latch Disabled); Disabled Outputs
H H	L L	h l	Z Z	Latched (Latch Enabled); Disabled Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition; NC = No Change, State Prior to the Latch Enable High–to–Low Transition; X = High or Low Voltage Level or Transitions are Acceptable; Z = High Impedance State; For I_{CC} Reasons DO NOT FLOAT Inputs

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = –50µA I_{OH} = –50µA I_{OH} = –4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50µA I_{OL} = 50µA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.25		±2.5	µA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay LE to O	$V_{CC} = 2.7V$	$C_L = 15pF$		8.2	15.6	1.0	18.5	ns
			$C_L = 50pF$		10.7	19.1	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$		6.4	10.1	1.0	12.0	
			$C_L = 50pF$		8.9	13.6	1.0	15.5	
t_{PLH}, t_{PHL}	Propagation Delay D to O	$V_{CC} = 2.7V$	$C_L = 15pF$		7.6	14.5	1.0	17.5	ns
			$C_L = 50pF$		10.1	18.0	1.0	21.0	
		$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$		5.9	9.3	1.0	11.0	
			$C_L = 50pF$		8.4	12.8	1.0	14.5	
t_{PZL}, t_{PZH}	Output Enable Time OE to O	$V_{CC} = 2.7V$, $R_L = 1k\Omega$	$C_L = 15pF$		7.8	15.0	1.0	18.5	ns
			$C_L = 50pF$		10.3	18.5	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3V$, $R_L = 1k\Omega$	$C_L = 15pF$		6.1	9.7	1.0	12.0	
			$C_L = 50pF$		8.6	13.2	1.0	15.5	
t_{PLZ}, t_{PHZ}	Output Disable Time OE to O	$V_{CC} = 2.7V$, $R_L = 1k\Omega$	$C_L = 50pF$		12.1	19.1	1.0	22.0	ns
		$V_{CC} = 3.3 \pm 0.3V$, $R_L = 1k\Omega$	$C_L = 50pF$		10.1	13.6	1.0	15.5	
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1.)	$V_{CC} = 2.7V$	$C_L = 50pF$			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3V$	$C_L = 50pF$			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2.)		29				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50pF$, $V_{CC} = 3.3V$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.5	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		6.5 5.0	7.5 5.0	ns
t_{su}	Minimum Setup Time, D to LE	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		5.0 3.5	5.0 3.5	ns
t_h	Minimum Hold Time, D to LE	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V		1.5 1.5	1.5 1.5	ns

SWITCHING WAVEFORMS

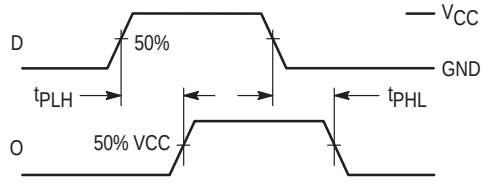


Figure 3.

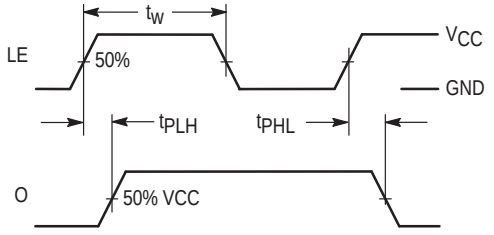


Figure 4.

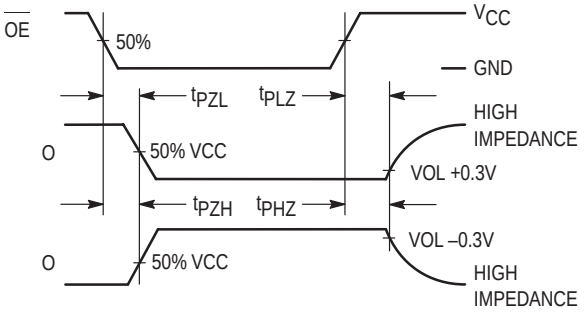


Figure 5.

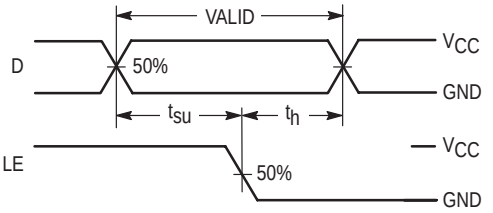
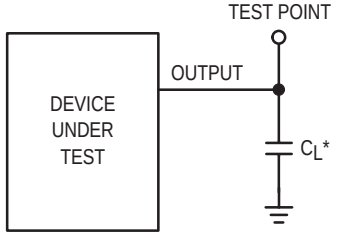


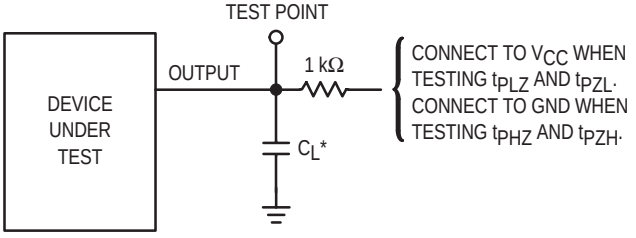
Figure 6.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 7. Propagation Delay Test Circuit



* Includes all probe and jig capacitance

Figure 8. Three–State Test Circuit

Dual Supply Translators

Advance Information

Configurable Dual Supply Octal Transceiver
with 3-State Outputs for 3V Systems

MC74LVXC3245

LVX

LOW–VOLTAGE CMOS

The 74LVXC3245 is a 24–pin dual–supply, octal configurable voltage interface transceiver especially well suited for PCMCIA and other real time configurable I/O applications. The V_{CCA} pin accepts a 3V supply level; the A port is a dedicated 3V port. The V_{CCB} pin accepts a 3V–to–5V supply level. The B port is configured to track the V_{CCB} supply level. A 5V level on the V_{CCB} pin will configure the I/O pins at a 5V level and a 3V V_{CCB} will configure the I/O pins at a 3V level. The A port interfaces with a 3V host system and the B port to the card slots. This device will allow the V_{CCB} voltage source pin and I/O pins on the B port to float when OE is High. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation. The Transmit/Receive (T/R) input determines the direction of data flow. Transmit (active–High) enables data from the A port to B port. Receive (active–Low) enables data from the B port to the A port.

- Bidirectional Interface Between 3V and 3V/5V Buses
- Control Inputs Compatible with TTL Level
- Outputs Source/Sink Up to 24mA
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Available in SOIC and TSSOP Packages
- Flexible V_{CCB} Operating Range
- Allows B Port and V_{CCB} to Float Simultaneously When $\overline{OE}$ Is High
- Functionally Compatible with the 74 Series 245

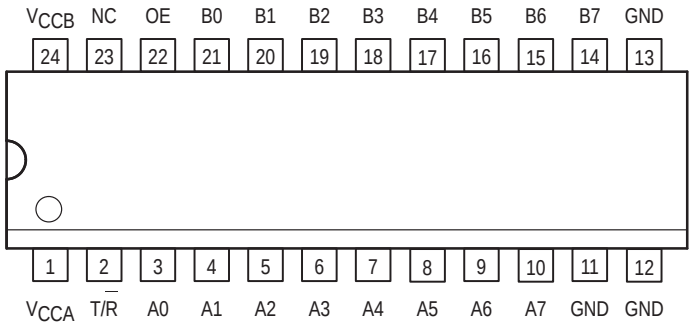
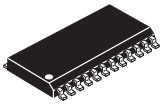
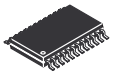


Figure 1. 24–Lead Pinout (Top View)



DW SUFFIX
24–LEAD PLASTIC WIDE SOIC PACKAGE
CASE 751E–04



DT SUFFIX
24–LEAD PLASTIC TSSOP PACKAGE
CASE 948H–01

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
T/R	Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State Outputs
B0–B7	Side B 3–State Inputs or 3–State Outputs

This document contains information on a new product. Specifications and information herein are subject to change without notice.

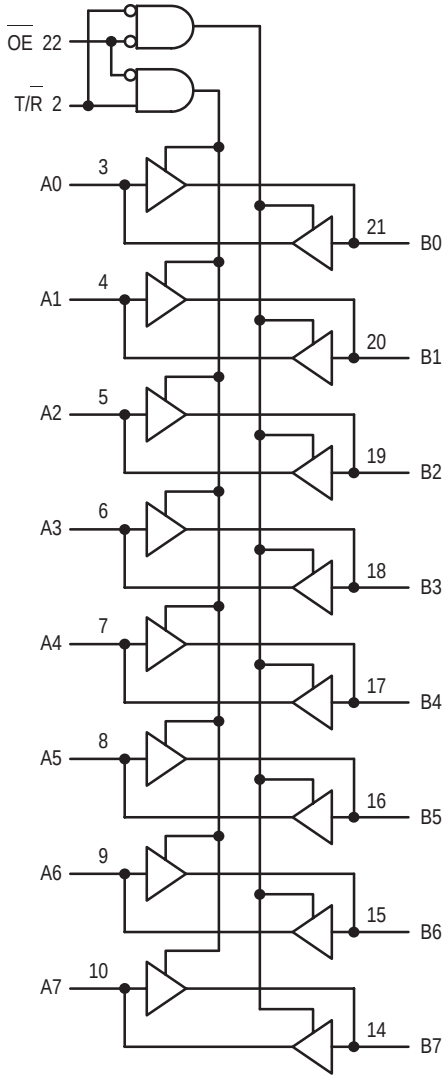


Figure 2. Logic Diagram

INPUTS		OPERATING MODE Non–Inverting
OE	T/R	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		–0.5 to +7.0		V
V_I	DC Input Voltage	$\overline{OE}$, T/$\overline{R}$	–0.5 to V_{CCA} +0.5		V
$V_{I/O}$	DC Input/Output Voltage	An	–0.5 to V_{CCA} +0.5		V
		Bn	–0.5 to V_{CCB} +0.5		V
I_{IK}	DC Input Diode Current	$\overline{OE}$, T/$\overline{R}$	±20	V_I < GND	mA
I_{OK}	DC Output Diode Current		±50	V_O < GND; V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CC}, I_{GND}	DC Supply Current	Per Output Pin Maximum Current	±50 ±200		mA
T_{STG}	Storage Temperature Range		–65 to +150		°C
	DC Latchup Source/Sink Current		±300		mA

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Supply Voltage ($V_{CCA} \le V_{CCB}$)	V_{CCA} V_{CCB}	2.7 3.0	3.6 5.5	V
V_I	Input Voltage	$\overline{OE}$, T/$\overline{R}$	0	V_{CCA}	V
$V_{I/O}$	Input/Output Voltage	An Bn	0 0	V_{CCA} V_{CCB}	V
T_A	Operating Free–Air Temperature		–40	+85	°C
$\Delta t/\Delta V$	Minimum Input Edge Rate V_{IN} from 30% to 70% of V_{CC}; V_{CC} at 3.0V, 4.5V, 5.5V		0	8	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V_{CCA}	V_{CCB}	T_A = 25°C	T_A = –40 to +85°C		Unit
						Typ	Guaranteed Limits		
V_{IHA}	Minimum HIGH Level Input Voltage	$\overline{An}$ $\overline{OE}$ T/$\overline{R}$	$V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$	2.7 3.0 3.6	3.0 3.6 5.5		2.0 2.0 2.0	2.0 2.0 2.0	V
V_{IHB}		Bn		2.7 3.0 3.6	3.0 3.6 5.5		2.00 2.00 3.85	2.00 2.00 3.85	V
V_{ILA}	Maximum LOW Level Input Voltage	$\overline{An}$ $\overline{OE}$ T/$\overline{R}$	$V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$	2.7 3.0 3.6	3.0 3.6 5.5		0.8 0.8 0.8	0.8 0.8 0.8	V
V_{ILB}		Bn		2.7 3.0 3.6	3.0 3.6 5.5		0.80 0.80 1.65	0.80 0.80 1.65	V
V_{OHA}	Minimum HIGH Level Output Voltage		I_{OUT} = –100µA I_{OH} = –12mA I_{OH} = –24mA I_{OH} = –12mA I_{OH} = –24mA	3.0 3.0 3.0 2.7 2.7	3.0 3.0 3.0 3.0 4.5	2.99 2.85 2.65 2.50 2.30	2.90 2.56 2.35 2.30 2.10	2.90 2.46 2.25 2.20 2.00	V
V_{OHB}			I_{OUT} = –100µA I_{OH} = –12mA I_{OH} = –24mA I_{OH} = –24mA	3.0 3.0 3.0 3.0	3.0 3.0 3.0 4.5	2.99 2.85 2.65 4.25	2.90 2.56 2.35 3.86	2.90 2.46 2.25 3.76	V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V_{CCA}	V_{CCB}	T_A = 25°C	T_A = –40 to +85°C		Unit
						Typ	Guaranteed Limits		
V_{OLA}	Maximum LOW Level Output Voltage		I_{OUT} = 100μA I_{OL} = 24mA I_{OL} = 12mA I_{OL} = 24mA	3.0 3.0 2.7 2.7	3.0 3.0 3.0 4.5	0.002 0.21 0.11 0.22	0.10 0.36 0.36 0.42	0.10 0.44 0.44 0.50	V
V_{OLB}			I_{OUT} = 100μA I_{OL} = 24mA I_{OL} = 24mA	3.0 3.0 3.0	3.0 3.0 4.5	0.002 0.21 0.18	0.10 0.36 0.36	0.10 0.44 0.44	V
I_{IN}	Max Input Leakage Current	$\overline{OE}$, T/R	$V_I = V_{CCA}$, GND	3.6 3.6	3.6 5.5		±0.1 ±0.1	±1.0 ±1.0	μA
I_{OZA}	Max 3–State Output Leakage	An	$V_I = V_{IH}, V_{IL}$ OE = V_{CCA} $V_O = V_{CCA}$, GND	3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA
I_{OZB}	Max 3–State Output Leakage	Bn	$V_I = V_{IH}, V_{IL}$ OE = V_{CCA} $V_O = V_{CCB}$, GND	3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA
ΔI_{CC}	Maximum I_{CC}/Input	Bn	$V_I = V_{CCB} – 2.1V$	3.6	5.5	1.0	1.35	1.5	mA
		All Inputs	$V_I = V_{CC} – 0.6V$	3.6	3.6		0.35	0.5	mA
I_{CCA1}	Quiescent V_{CCA} Supply Current as B Port Floats		An=V_{CCA} or GND Bn=Open, OE=V_{CCA}, T/R=V_{CCA}, V_{CCB}=Open	3.6	Open		5	50	μA
I_{CCA2}	Quiescent V_{CCA} Supply Current		An=V_{CCA} or GND Bn=V_{CCB} or GND, OE=GND, T/R=GND	3.6 3.6	3.6 5.5		5 5	50 50	μA
I_{CCB}	Quiescent V_{CCB} Supply Current		An=V_{CCA} or GND Bn=V_{CCB} or GND, OE=GND, T/R=V_{CCA}	3.6 3.6	3.6 5.5		5 8	50 80	μA
V_{OLPA}	Quiet Output Max Dynamic V_{OL}		Notes 1., 2.	3.3 3.3	3.3 5.0		0.8 0.8		V
V_{OLPB}			Notes 1., 2.	3.3 3.3	3.3 5.0		0.8 1.5		V
V_{OLVA}	Quiet Output Min Dynamic V_{OL}		Notes 1., 2.	3.3 3.3	3.3 5.0		–0.8 –0.8		V
V_{OLVB}			Notes 1., 2.	3.3 3.3	3.3 5.0		–0.8 –1.2		V
V_{IHDA}	Min HIGH Level Dynamic Input Voltage		Notes 1., 3.	3.3 3.3	3.3 5.0		2.0 2.0		V
V_{IHDB}			Notes 1., 3.	3.3 3.3	3.3 5.0		2.0 3.5		V
V_{ILDA}	Max LOW Level Dynamic Input Voltage		Notes 1., 3.	3.3 3.3	3.3 5.0		0.8 0.8		V
V_{ILDB}			Notes 1., 3.	3.3 3.3	3.3 5.0		0.8 1.5		V

1. Worst case package.
2. Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.
3. Max number of data inputs (n) switching. (n–1) inputs switching 0V to V_{CC} level. Input under test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1MHz.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = –40 to +85°C; C_L = 50pF						Unit
		V_{CCA} = 2.7–3.6V V_{CCB} = 4.5–5.5V			V_{CCA} = 2.7–3.6V V_{CCB} = 3.0–3.6V			
		Min	Typ (Note 4.)	Max	Min	Typ (Note 5.)	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0 1.0	4.8 3.9	8.5 7.0	1.0 1.0	5.5 5.2	9.0 8.5	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0 1.0	3.8 4.3	7.0 8.0	1.0 1.0	4.4 5.1	7.5 8.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0 1.0	4.7 4.8	8.5 9.0	1.0 1.0	6.0 6.1	9.5 10.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0 1.0	5.9 5.4	10.0 9.5	1.0 1.0	6.4 5.8	10.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0 1.0	4.0 3.8	8.5 8.0	1.0 1.0	6.3 4.5	10.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	1.0 1.0	4.6 3.1	10.0 7.0	1.0 1.0	5.2 3.4	10.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew, Data to Output (Note 5.)		1.0	1.5		1.0	1.5	ns

4. Typical values at V_{CCA} = 3.3V, V_{CCB} = 5.0V at 25°C.
5. Typical values at V_{CCA} = 3.3V, V_{CCB} = 3.3V at 25°C.
6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CCA} = 3.3V; V_{CCB} = 5.0V	4.5	pF
$C_{I/O}$	Input/Output Capacitance	V_{CCA} = 3.3V; V_{CCB} = 5.0V	10	pF
C_{PD}	Power Dissipation Capacitance (Measured at 10MHz) A B B A	V_{CCB} = 5.0V V_{CCA} = 3.3V	50 40	pF

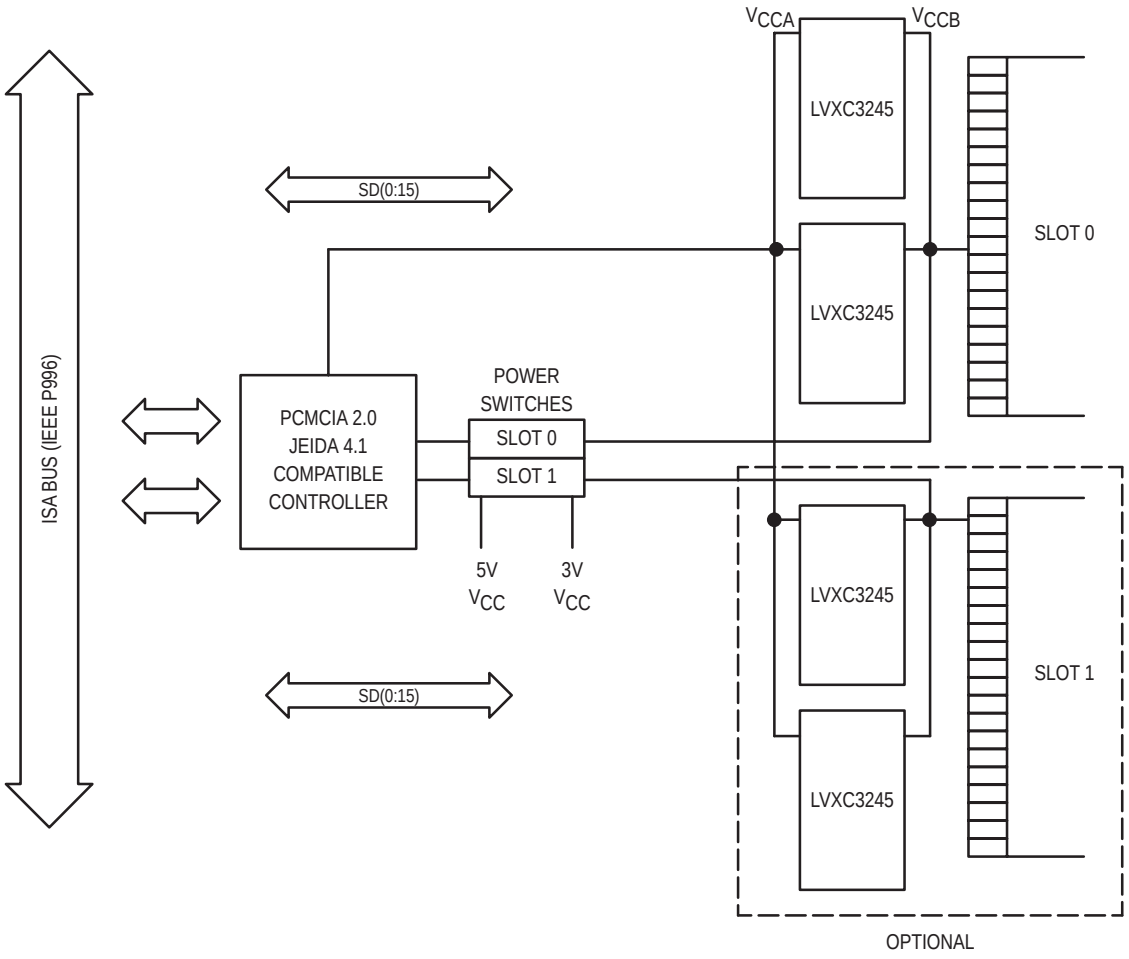
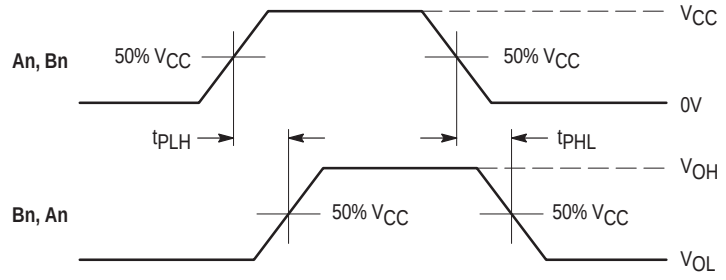


Figure 3. Block Diagram

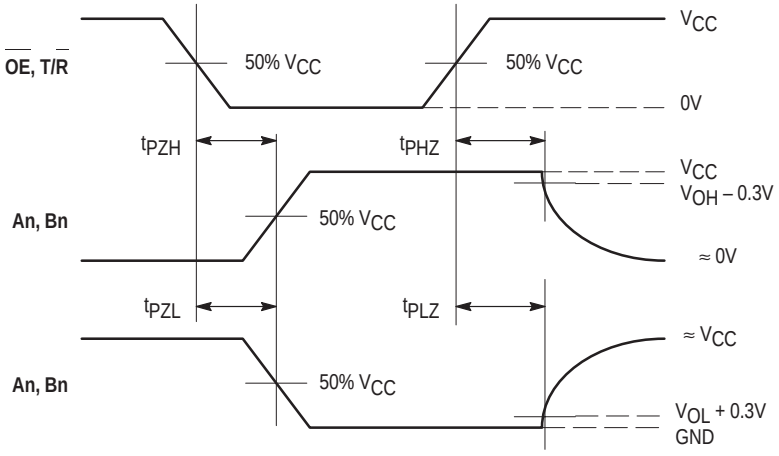
Configurable I/O Application for PCMCIA Cards

The 74LVXC3245 is a dual–supply device well suited for PCMCIA configurable I/O applications. The LVXC3245 consumes less than 1mW of quiescent power in all modes of operation, making it ideal for low power notebook designs. The LVXC3245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying the V_{CCB} pin to the card voltage supply, the PCMCIA card will always have rail–to–rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin must always be tied to a 3.3V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the figure above, the LVXC3245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

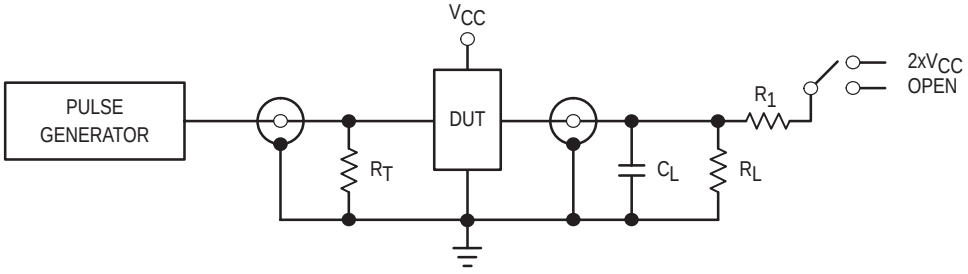


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 4. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2xV_{CC}

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5. Test Circuit

Dual Supply Octal Translating Transceiver
with 3-State Outputs

MC74LVX4245

LVX

LOW–VOLTAGE CMOS

The 74LVX4245 is a 24–pin dual–supply, octal translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment such as laptop computers using a 3.3V CPU and 5V LCD display. The A port interfaces with the 5V bus; the B port interfaces with the 3V bus.

The Transmit/Receive (T/R) input determines the direction of data flow. Transmit (active–High) enables data from the A port to the B port. Receive (active–Low) enables data from the B port to the A port. The Output Enable (OE) input, when High, disables both A and B ports by placing them in 3–State.

- Bi–directional Interface Between 5V and 3V Buses
- Control Inputs Compatible with TTL Level
- 5V Data Flow at A Port and 3V Data Flow at B Port
- Outputs Source/Sink 24mA at 5V Bus and 12mA at 3V Bus
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Available in SOIC and TSSOP Packages
- Functionally Compatible with the 74 Series 245

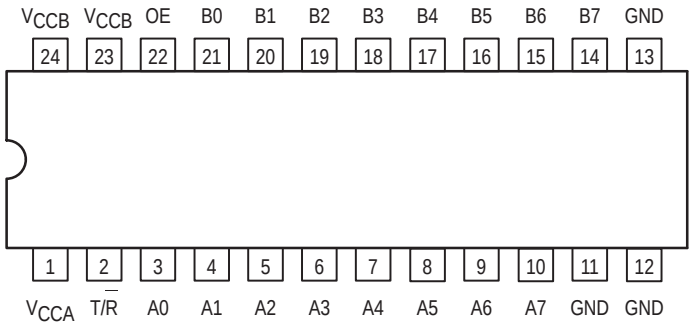
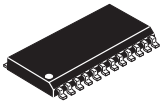
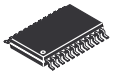


Figure 1. 24–Lead Pinout
(Top View)



DW SUFFIX
24–LEAD PLASTIC SOIC PACKAGE
CASE 751E–04



DT SUFFIX
24–LEAD PLASTIC TSSOP PACKAGE
CASE 948H–01

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
T/R	Transmit/Receive Input
A0–A7	Side A 3–State Inputs or 3–State Outputs
B0–B7	Side B 3–State Inputs or 3–State Outputs

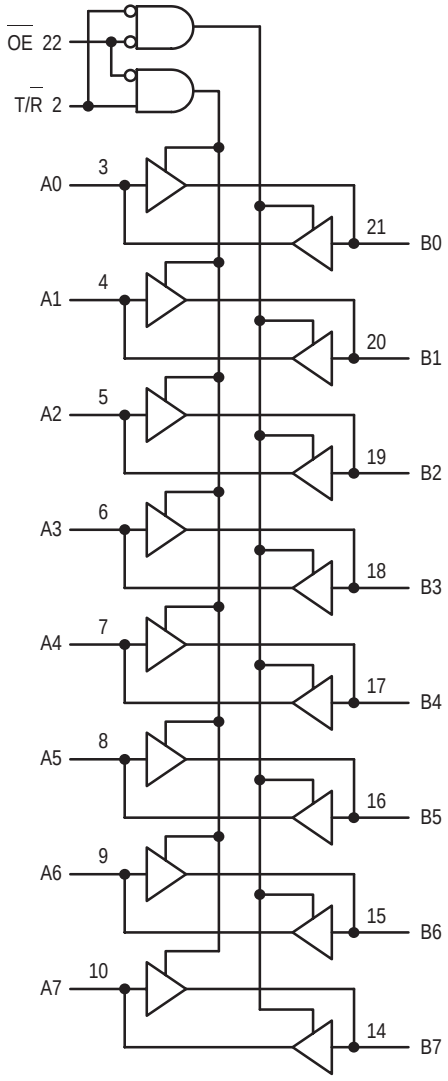


Figure 2. Logic Diagram

INPUTS		OPERATING MODE Non–Inverting
OE	T/R	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		–0.5 to +7.0		V
V_I	DC Input Voltage	$\overline{OE}$, T/$\overline{R}$	–0.5 to V_{CCA} +0.5		V
$V_{I/O}$	DC Input/Output Voltage	An	–0.5 to V_{CCA} +0.5		V
		Bn	–0.5 to V_{CCB} +0.5		V
I_{IK}	DC Input Diode Current	$\overline{OE}$, T/$\overline{R}$	±20	V_I < GND	mA
I_{OK}	DC Output Diode Current		±50	V_O < GND; V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CC}, I_{GND}	DC Supply Current	Per Output Pin Maximum Current at I_{CCA} Maximum Current at I_{CCB}	±50 ±200 ±100		mA
T_{STG}	Storage Temperature Range		–65 to +150		°C
Latchup	DC Latchup Source/Sink Current		±300		mA

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Supply Voltage	V_{CCA} V_{CCB}	4.5 2.7	5.5 3.6	V
V_I	Input Voltage	$\overline{OE}$, T/$\overline{R}$	0	V_{CCA}	V
$V_{I/O}$	Input/Output Voltage	An Bn	0 0	V_{CCA} V_{CCB}	V
T_A	Operating Free–Air Temperature		–40	+85	°C
$\Delta t/\Delta V$	Minimum Input Edge Rate V_{IN} from 30% to 70% of V_{CC}; V_{CC} at 3.0V, 4.5V, 5.5V		0	8	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V_{CCA}	V_{CCB}	T_A = 25°C	T_A = –40 to +85°C		Unit
						Typ	Guaranteed Limits		
V_{IHA}	Minimum HIGH Level Input Voltage	An, $\overline{OE}$ T/$\overline{R}$	V_{OUT} ≤ 0.1V or ≥ V_{CC} – 0.1V	5.5 4.5	3.3 3.3		2.0 2.0	2.0 2.0	V
V_{IHB}		Bn		5.0 5.0	3.6 2.7		2.0 2.0	2.0 2.0	V
V_{ILA}	Maximum LOW Level Input Voltage	An, $\overline{OE}$ T/$\overline{R}$	V_{OUT} ≤ 0.1V or ≥ V_{CC} – 0.1V	5.5 4.5	3.3 3.3		0.8 0.8	0.8 0.8	V
V_{ILB}		Bn		5.0 5.0	2.7 3.6		0.8 0.8	0.8 0.8	V
V_{OHA}	Minimum HIGH Level Output Voltage		I_{OUT} = –100µA I_{OH} = –24mA	4.5 4.5	3.0 3.0	4.50 4.25	4.40 3.86	4.40 3.76	V
V_{OHB}			I_{OUT} = –100µA I_{OH} = –12mA I_{OH} = –8mA	4.5 4.5 4.5	3.0 3.0 2.7	2.99 2.80 2.50	2.9 2.4 2.4	2.9 2.4 2.4	V
V_{OLA}	Maximum LOW Level Output Voltage		I_{OUT} = 100µA I_{OL} = 24mA	4.5 4.5	3.0 3.0	0.002 0.18	0.10 0.36	0.10 0.44	V
V_{OLB}			I_{OUT} = 100µA I_{OL} = 12mA I_{OL} = 8mA	4.5 4.5 4.5	3.0 3.0 2.7	0.002 0.1 0.1	0.10 0.31 0.31	0.10 0.40 0.40	V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V_{CCA}	V_{CCB}	T_A = 25°C	T_A = –40 to +85°C		Unit
						Typ	Guaranteed Limits		
I_{IN}	Max Input Leakage Current	$\overline{OE}$, T/R	V_I = V_{CCA}, GND	5.5	3.6		±0.1	±1.0	μA
I_{OZA}	Max 3–State Output Leakage	An	V_I = V_{IH}, V_{IL} OE = V_{CCA} V_O = V_{CCA}, GND	5.5	3.6		±0.5	±5.0	μA
I_{OZB}	Max 3–State Output Leakage	Bn	V_I = V_{IH}, V_{IL} OE = V_{CCA} V_O = V_{CCB}, GND	5.5	3.6		±0.5	±5.0	μA
ΔI_{CC}	Maximum I_{CCT} per Input	An, $\overline{OE}$, T/R	V_I=V_{CCA}–2.1V	5.5	3.6	1.0	1.35	1.5	mA
		Bn	V_I=V_{CCB}–0.6V	5.5	3.6		0.35	0.5	mA
I_{CCA}	Quiescent V_{CCA} Supply Current		An=V_{CCA} or GND Bn=V_{CCB} or GND OE=GND T/R=GND	5.5	3.6		8	80	μA
I_{CCB}	Quiescent V_{CCB} Supply Current		An=V_{CCA} or GND Bn=V_{CCB} or GND OE=GND T/R=V_{CCA}	5.5	3.6		5	50	μA
V_{OLPA} V_{OLPB}	Quiet Output Max Dynamic V_{OL}		Notes 1., 2.	5.0 5.0	3.3 3.3		1.5 1.2		V
V_{OLVA} V_{OLVB}	Quiet Output Min Dynamic V_{OL}		Notes 1., 2.	5.0 5.0	3.3 3.3		–1.2 –0.8		V
V_{IHDA} V_{IHDB}	Min HIGH Level Dynamic Input Voltage		Notes 1., 3.	5.0 5.0	3.3 3.3		2.0 2.0		V
V_{ILDA} V_{ILDB}	Max LOW Level Dynamic Input Voltage		Notes 1., 3.	5.0 5.0	3.3 3.3		0.8 0.8		V

1. Worst case package.
2. Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.
3. Max number of data inputs (n) switching. (n–1) inputs switching 0V to V_{CC} level. Input under test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1MHz.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter		Condition	Typical	Unit
C_{IN}	Input Capacitance		V_{CCA} = 5.0V; V_{CCB} = 3.3V	4.5	pF
$C_{I/O}$	Input/Output Capacitance		V_{CCA} = 5.0V; V_{CCB} = 3.3V	15	pF
C_{PD}	Power Dissipation Capacitance (Measured at 10MHz)	B A A B	V_{CCA} = 5.0V V_{CCB} = 3.3V	55 40	pF

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = –40 to +85°C, C_L = 50pF, V_{CCA} = 5V ±0.5V, V_{CCB} = 3.3V ±0.3V			T_A = –40 to +85°C, C_L = 50pF, V_{CCA} = 5V ±0.5V, V_{CCB} = 2.7V		Unit
		Min	Typ (Note 4.)	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0 1.0	5.1 5.3	9.0 9.0	1.0 1.0	10.0 10.0	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0 1.0	5.4 5.5	9.0 9.0	1.0 1.0	10.0 10.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0 1.0	6.5 6.7	10.5 10.5	1.0 1.0	11.5 11.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0 1.0	5.2 5.8	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0 1.0	6.0 3.3	10.0 7.0	1.0 1.0	10.0 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	1.0 1.0	3.9 2.9	7.5 7.0	1.0 1.0	7.5 7.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew, Data to Output (Note 5.)		1.0	1.5		1.5	ns

4. Typical values at V_{CCA} = 5.0V; V_{CCB} = 3.3V at 25°C.
5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

Dual Supply Octal Translating Transceiver

The 74LVX4245 is a is a dual–supply device well capable of bidirectional signal voltage translation. This level shifting ability provides an excellent interface between low voltage CPU local bus and a standard 5V I/O bus. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

The LVX4245 is ideal for mixed voltage applications such as notebook computers using a 3.3V CPU and 5V peripheral devices.

Applications:
Mixed Mode Dual Supply Interface Solutions

The LVX4245 is designed to solve 3V/5V interfaces when CMOS devices cannot tolerate I/O levels above their applied V_{CC}. If an I/O pin of a 3V device is driven by a 5V device, the P–Channel transistor in the 3V device will conduct — causing current flow from the I/O bus to the 3V power supply. The result may be destruction of the 3V device through latchup effects. A current limiting resistor may be used to prevent destruction, but it causes speed degradation and needless power dissipation.

A better solution is provided in the LVX4245. It provides two different output levels that easily handle the dual voltage interface. The A port is a dedicated 5V port; the B port is a dedicated 3V port. Figure 4 on page 82 shows how the LVX4245 may fit into a mixed 3V/5V system.

Since the LVX4245 is a ‘245 transceiver, the user may either use it for bidirectional or unidirectional applications. The center 20 pins are configured to match a ‘245 pinout. This enables the user to easily replace this level shifter with a 3V ‘245 device without additional layout work or re–manufacture of the circuit board (when both buses are 3V).

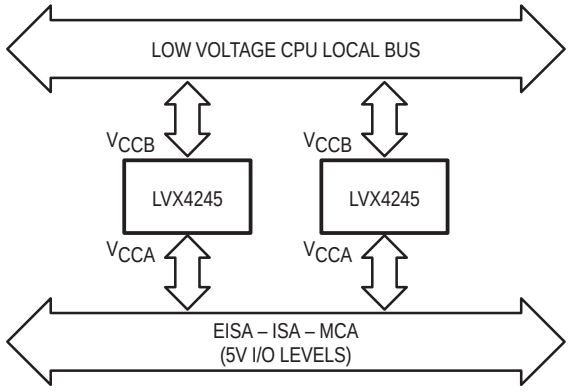


Figure 3. 3.3V/5V Interface Block Diagram

Powering Up the LVX4245

When powering up the LVX4245, please note that if the V_{CCB} pin is powered–up well in advance of the V_{CCA} pin, several milliamps of either I_{CCA} or I_{CCB} current will result. If the V_{CCA} pin is powered–up in advance of the V_{CCB} pin then only nanoamps of Icc current will result. In actuality the V_{CCB} can be powered “slightly” before the V_{CCA} without the current penalty, but this “setup time” is dependent on the power–up ramp rate of the V_{CC} pins. With a ramp rate of approximately 50mV/ns (50V/μs) a 25ns setup time was observed (V_{CCB}

before V_{CCA}). With a 7V/µs rate, the setup time was about 140ns. When all is said and done, the safest power–up strategy is to simply power V_{CCA} before V_{CCB}. One more note: if the V_{CCB} ramp rate is faster than the V_{CCA} ramp rate then power problems might still occur, even if the V_{CCA} power–up began prior to the V_{CCB} power–up.

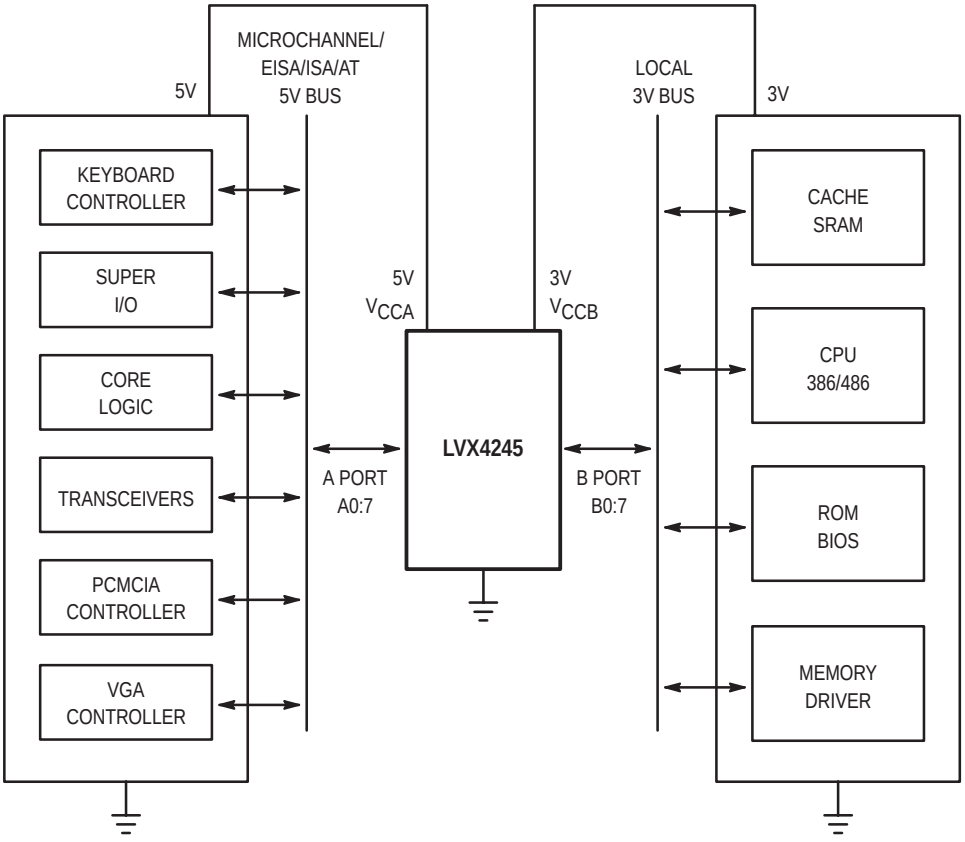


Figure 4. MC74LVX4245 Fits Into a System with 3V Subsystem and 5V Subsystem

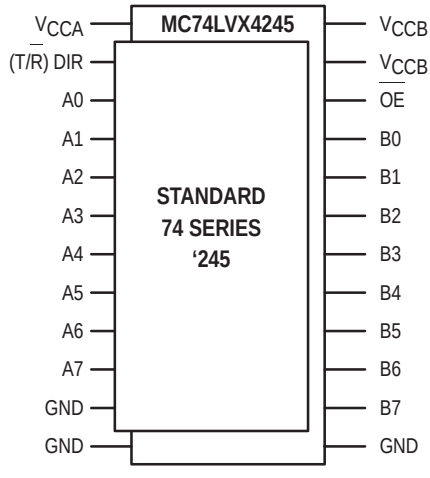
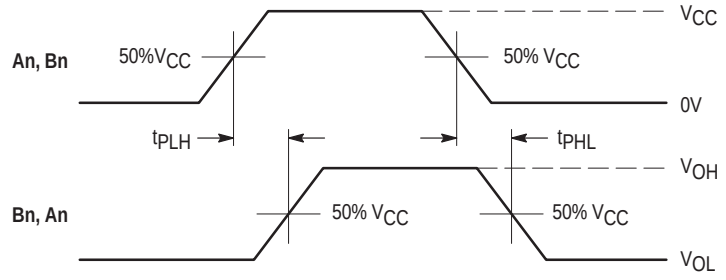
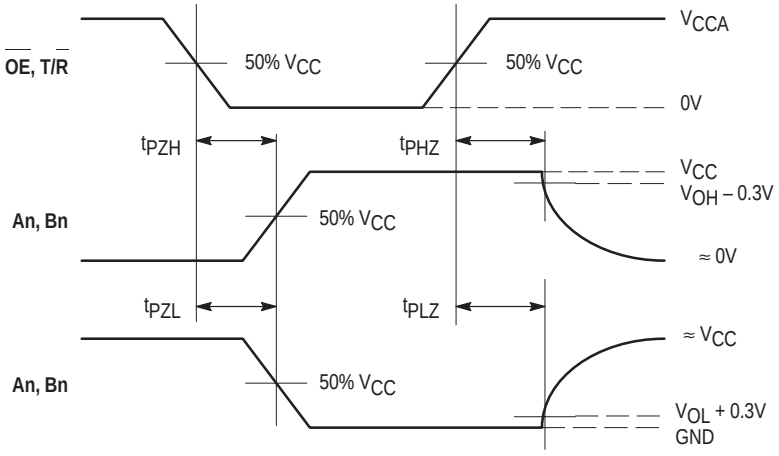


Figure 5. MC74LVX4245 Pin Arrangement Is Compatible to 20–Pin 74 Series ‘245s

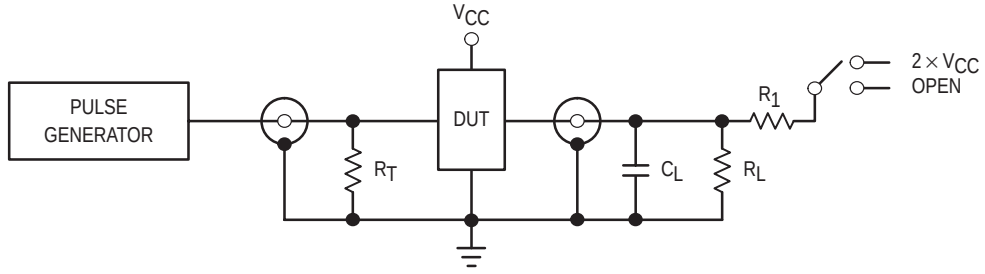


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 6. AC Waveforms



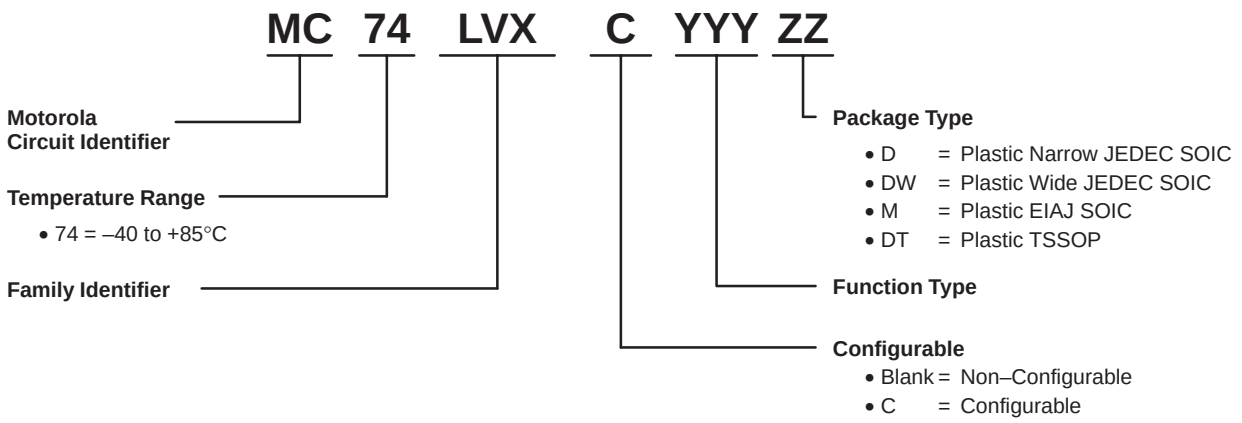
TEST	SWITCH
t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 × V_{CC}

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 7. Test Circuit

Ordering Information

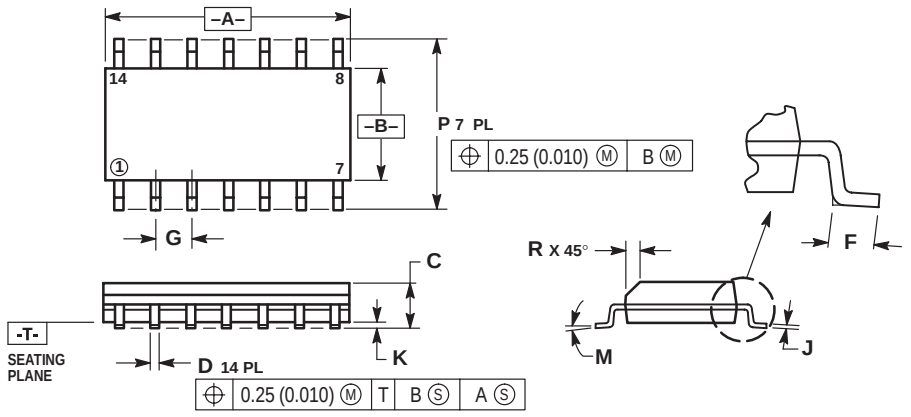
Device Nomenclature



Case Outlines

14-Pin Packages

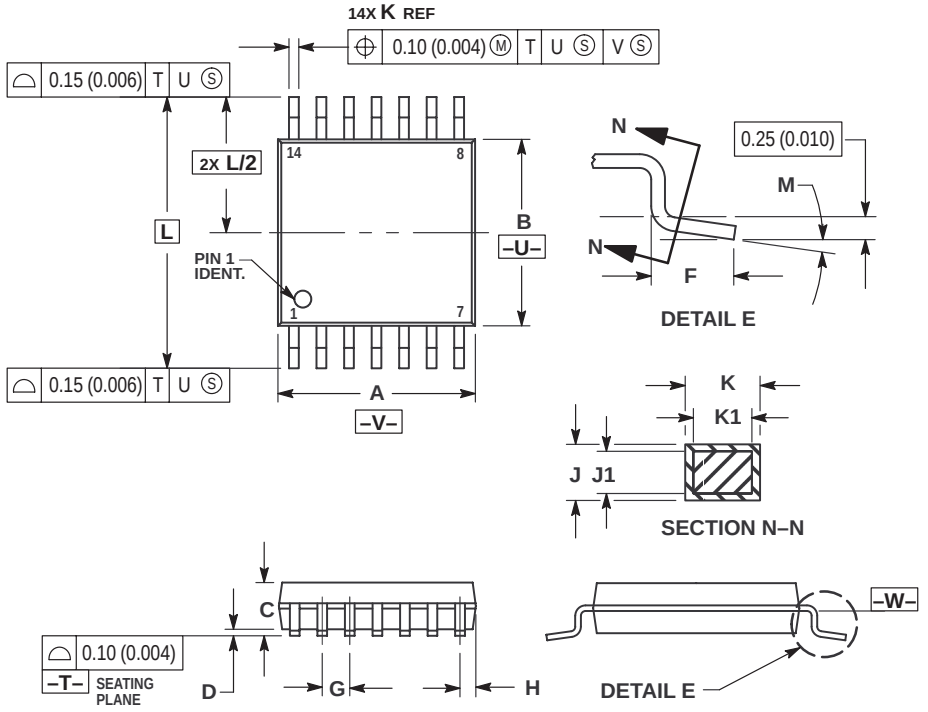
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O

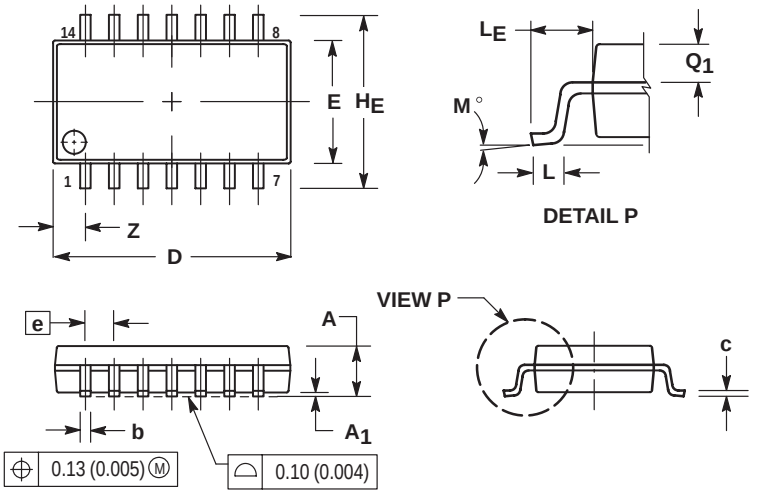


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

14-Pin Packages (continued)

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O

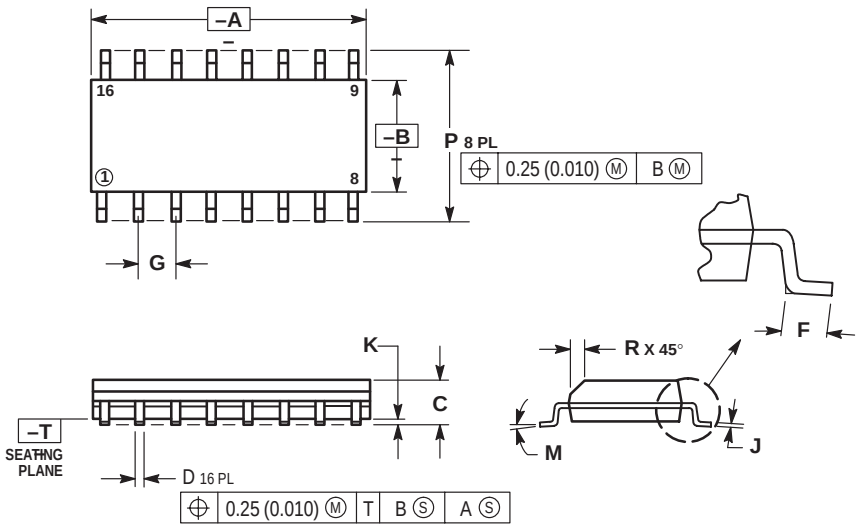


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

16-Pin Packages

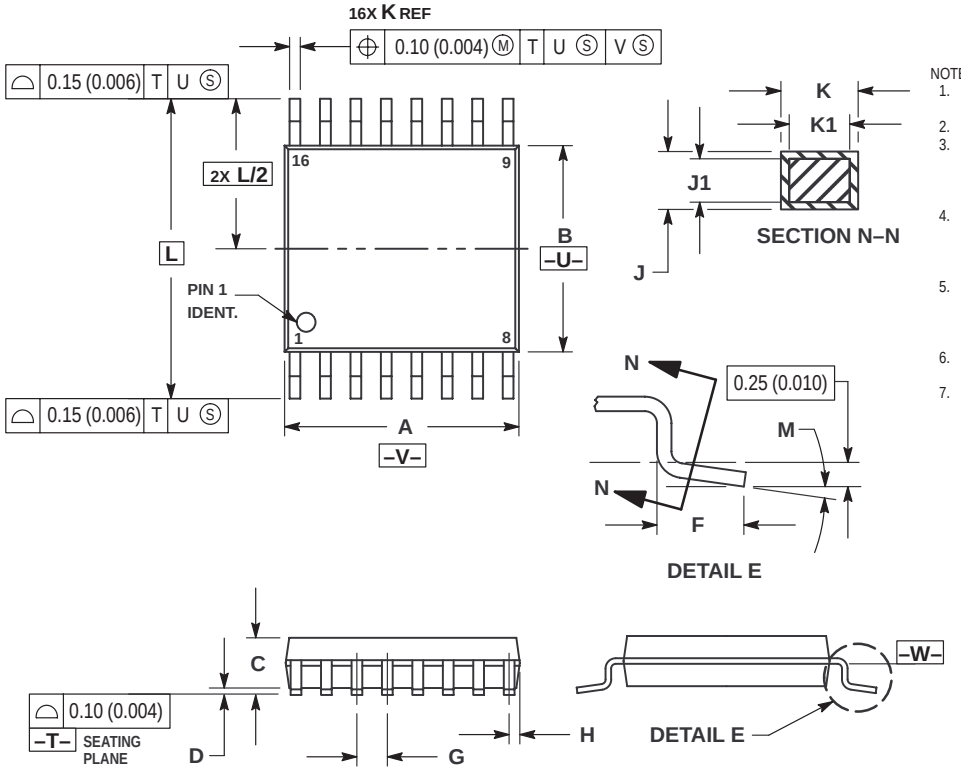
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O

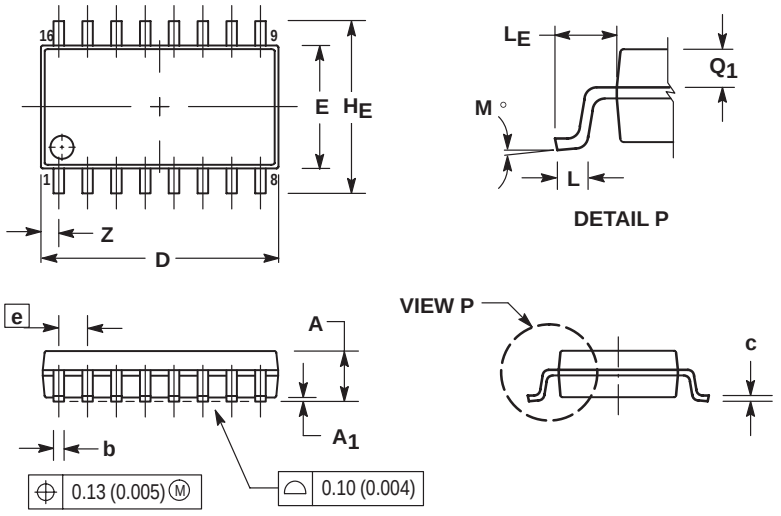


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

16-Pin Packages (continued)

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 966–01
ISSUE O

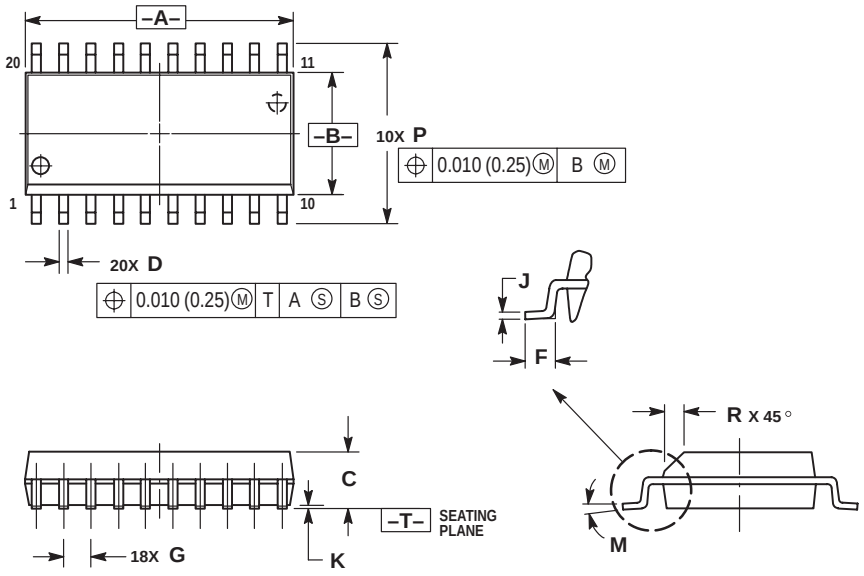


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

20-Pin Packages

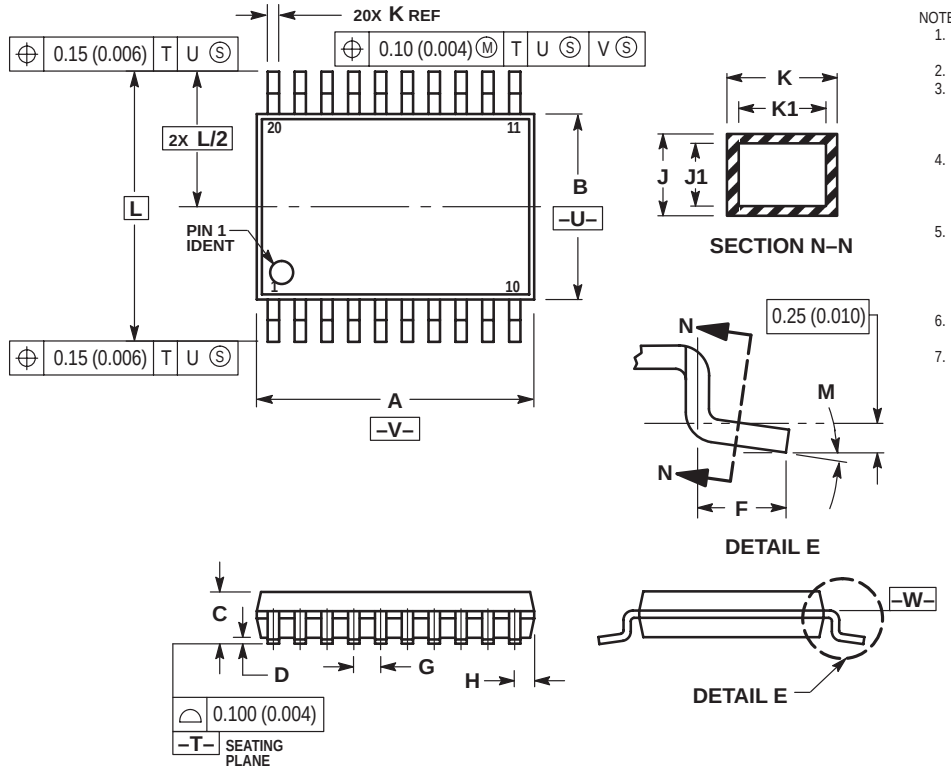
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A

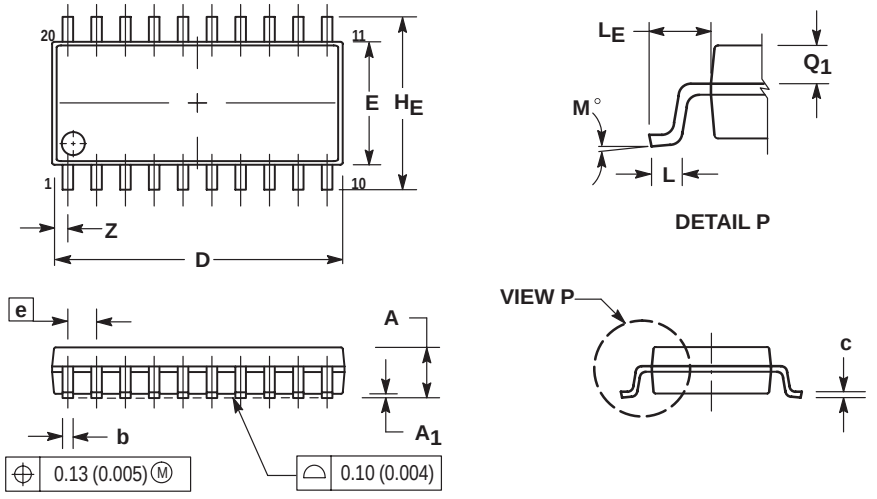


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

20-Pin Packages (continued)

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967–01
ISSUE O

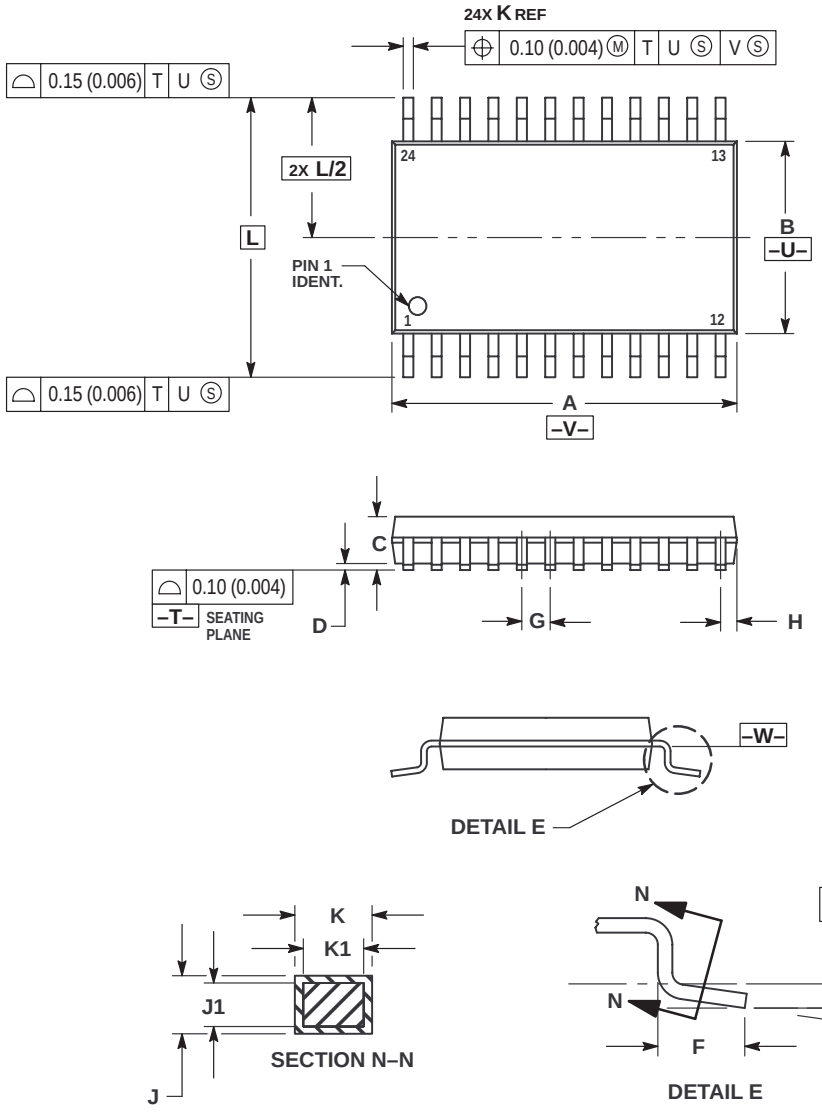


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	0.81	—	0.032

24-Pin Packages

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948H–01
ISSUE O

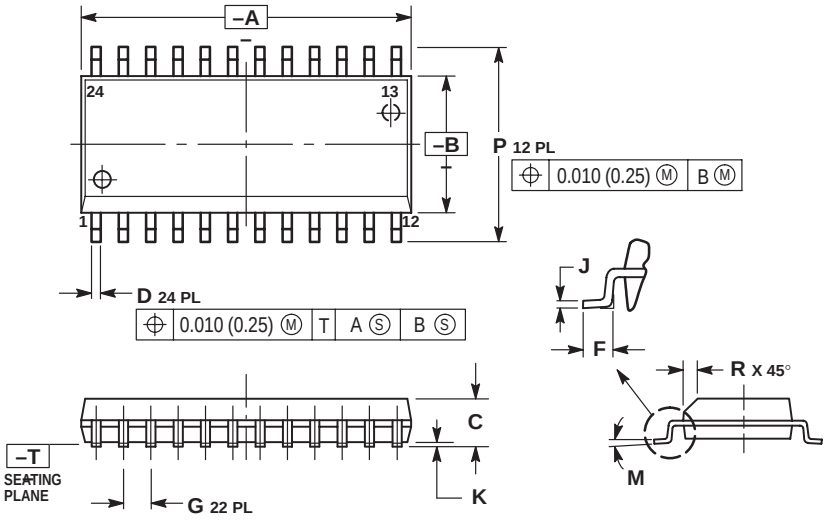


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

24-Pin Packages (continued)

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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